Curriculum Vitæ

Jordi Cortadella

November 11, 2024

Summary

Jordi Cortadella is a Full Professor of the Department of Computer Science at the *Universitat Politècnica de Catalunya* (Barcelona, Spain). He is a Fellow of the IEEE and member of the Academia Europaea.

He obtained his Ph.D. in Computer Science in 1987, at the same University. In 1988, he was a Visiting Scholar at the University of California, Berkeley. He has also been a visiting professor in Intel Corporation (Hillsboro, USA) in summer 1998 and summer 2001 and in Theseus Logic (Sunnyvale, USA) in summer 2000. He co-founded Elastix Corporation in 2007, a company producing EDA tools for asynchronous design.

His main research interests include formal methods and computer-aided design of VLSI systems, with special emphasis on asynchronous circuits. He has co-authored over 200 papers in technical journals and conferences. He has served in the technical programme committee of numerous conferences in the area of Electronic Design Automation and concurrency. He was Program co-chair of ASYNC 2010 and ICATPN 2004. He is now Associate Editor of the IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems.

His research has had a relevant impact in the scientific community. As an example, he designed an arithmetic circuit for fast addition and comparison, published in 1992. This circuit drew the attention of several companies and was introduced in some components of different microprocessors.

His contributions in the area of the synthesis and analysis of concurrent systems have also had a tangible impact. One of his most cited papers proposes techniques for the analysis of Petri nets using symbolic methods.

Possibly, the most relevant work has been in the area of asynchronous circuits. He has been working on this subject since the early 90's in a tight collaboration with an international team. The activities in this area can be qualified as *basic research*, but the obtained results have raised the interest of many industrial and academic institutions. The most observable results of this research, a tool for the synthesis of asynchronous controllers called *petrify* (`www.cs.upc.edu/~jordicf/petrify`) is currently being used by many Universities for research and teaching activities. This impact is also manifested by a frequently cited paper in this area: *Petrify: a tool for manipulating concurrent specifications and synthesis of asynchronous controllers*, IEICE Trans. on Information and Systems, March 1997.

He has published numerous papers in international journals: *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, *Proceedings of the IEEE*, *IEEE Transactions on Computers*, *IEEE Transactions on VLSI*, etc. Most of the contributions in this area have been covered by the book

> J. Cortadella, M. Kishinevsky, A. Kondratyev, L. Lavagno and A. Yakovlev,
> *Logic synthesis of asynchronous controllers and interfaces*,
> Springer Verlag, 2002.

The impact of his research has also been recognized by the nomination as a finalist of the *Descartes Prize 2002* and four best paper awards at the *Design Automation Conference* (2004), *Int. Symp. on Advanced Research in Asynchronous Circuits and Systems* (2004 and 2016) and *Int. Conf. on Application of Concurrency to System Design* (2009). He also obtained a *Distinction* for the Promotion of the University Research by the Generalitat de Catalunya in 2003.

The relevance of his work has also been recognized by the invitation to give tutorials and talks in prestigious conferences. In 2013, he was invited to give two seminars at the Collège de France on his work about asynchronous and elastic circuits.

Besides the public funding obtained from National and European Projects, Jordi Cortadella has also been involved in technology transfer actions to important companies in the microelectronics area from United States, e.g., Intel Corporation, Cadence Design Systems and Theseus Logic.

Finally, research has been time-shared with several academic positions involving different management activitites in the University: Vicedean of the *Facultat d'Informàtica de Barcelona*, President of the Comission for the Evaluation and Selection of Academic Staff of the UPC, Member of the Comission of Ph.D. programs of the UPC, Coordinator of two Ph.D. programs (Computer Architecture and Software), etc.

Contents

1 Personal data

Name: Jordi Cortadella
Birthdate and birthplace: January 29th, 1962. Martorell, Spain.

University: Universitat Politècnica de Catalunya.
Departament: Computer Science.
Position: Catedràtic d'Universitat (Full professor).
Address: Campus Nord, mòdul Omega, office 242. 08034 Barcelona, Spain.
Phone: +34 934137854.
Homepage: http://www.cs.upc.edu/~jordicf

2 Academic degrees

- *Llicenciat en Informàtica* (B.S. in Computer Science),
  Facultat d'Informàtica de Barcelona (UPC). June 1985.
- *Llicenciat amb grau en Informàtica* (M.S. in Computer Science)
  Facultat d'Informàtica de Barcelona (UPC). February 1986.
  Qualification: Matrícula de Honor.
- *Doctor en Informàtica*, (Ph.D. in Computer Science)
  Facultat d'Informàtica de Barcelona (UPC). June 1987.
  Qualification: Apto "Cum Laude" by unanimity.

3 Honors and awards

- Fellow of the IEEE. January 2015.
- Member of the Academia Europaea. October 2013.
- Best paper award at the *Int. Symp. on Field Programmable Gate Arrays*, for the paper *Buffer Placement and Sizing for High-Performance Dataflow Circuits*. February 2020.
- Best paper award at the *Int. Symp. on Advanced Research in Asynchronous Circuits and Systems*, for the paper *Ring Oscillator Clocks and Margins*. May 2016.
- Best paper award at the *Int. Conference on Application of Concurrency to System Design (ACSD)*, for the paper *Scheduling synchronous elastic designs*. June 2009.
- Best paper award at the *Design Automation Conference*, for the paper *A Recursive Paradigm to Solve Boolean Relations*. June 2004.
- Best paper award at the *Int. Symp. on Advanced Research in Asynchronous Circuits and Systems*, for the paper *Handshake protocols for de-synchronization*. April 2004.
- Distinction for the Promotion of University Research, by the Generalitat de Catalunya (Distinció de la Generalitat per a la Promoció de la Recerca Universitària), 2003.
- Finalist of the *Descartes prize 2002*, with the project *New asynchronous circuits: towards cost-effective and less complicated designs.* Coordinator of the project. See the finalists here: `ec.europa.eu/research/science-awards/pdf/descartes_press_finalist_2002_en.pdf`
- Best Ph.D. thesis award, Universitat Politècnica de Catalunya, 1992.
- National Award for the best student in Computer Science, 1986. (1er. premio nacional de Terminación de Estudios en Informática).

4 Positions

4.1 Academic positions

Period	Position	Department
Oct. 1985 - May 1988	Assistant Professor	Computer Architecture (UPC)
June 1988 - June 1997	Associate Professor	Computer Architecture (UPC)
July 1997 - Oct. 1999	Associate Professor	Computer Science (UPC)
since Nov. 1999	Full Professor	Computer Science (UPC)

4.2 Industrial positions

In June 2007, Jordi Cortadella co-founded Elastix Corporation, a company offering solutions for energy-efficient circuits using asynchronous design techniques. From 2007 to 2010, he was the Chief Scientist of the company.

4.3 Visiting positions

July 1988 – December 1988: Visiting professor at the Electrical Engineering and Computer Science Department at the University of California, Berkeley.

July 1998 – September 1998: Visiting professor at the Strategic CAD Labs, Intel Corporation, Hillsboro, OR.

July 2000 – September 2000: Visiting professor at Theseus Logic Sunnyvale, CA.

July 2001 – September 2001: Visiting professor at the Strategic CAD Labs, Intel Corporation, Hillsboro, OR.

5 Thesis advisor

5.1 Ph.D. thesis advisor

[1] Alex Vidal-Obiols. "Algorithmic Techniques for Physical Design: Macro Placement and Under-the-Cell Routing". Co-advised with Jordi Petit. PhD thesis. Universitat Politècnica de Catalunya, Jan. 2020.

[2] Lucas Machado. "Logic Decomposition and Adaptive Clocking for the Optimization of Digital Circuits". PhD thesis. Universitat Politècnica de Catalunya, Feb. 2019.

[3] Alberto Moreno. "Synthesis of Variability-Tolerant Circuits with Adaptive Clocking". PhD thesis. Universitat Politècnica de Catalunya, Mar. 2019.

[4] Palkesh Jain. "Algorithms and Methodologies for Interconnect Reliability Analysis of Integrated Circuits". Co-advised with Sachin S. Sapatnekar. PhD thesis. Universitat Politècnica de Catalunya, May 2017.

[5] Javier de San Pedro. "Structure discovery techniques for circuit design and process model visualization". PhD thesis. Universitat Politècnica de Catalunya, Oct. 2017.

[6] Nikita Nikitin. "Automatic Synthesis and Optimization of Chip Multiprocessors". PhD thesis. Universitat Politècnica de Catalunya, Apr. 2013.

[7] Marc Galceran-Oms. "Automatic Pipelining of Elastic Systems". Co-advised with Mike Kishinevsky. PhD thesis. Universitat Politècnica de Catalunya, Sept. 2011.

[8] Dmitry Bufistov. "Performance Optimization of Elastic Systems". PhD thesis. Universitat Politècnica de Catalunya, Dec. 2010.

[9] Kyller Costa Gorgônio. "Towards the Automatic Synthesis of Asynchronous Communication Mechanisms". PhD thesis. Universitat Politècnica de Catalunya, Dec. 2010.

[10] David Bañeres. “Logic Synthesis Techniques for High-Speed Circuits”. Co-advised with Mike Kishinevsky. PhD thesis. Universitat Politècnica de Catalunya, Feb. 2008.

[11] Robert Clarisó. “Abstract Interpretation Techniques for the Verification of Timed Systems”. PhD thesis. Universitat Politècnica de Catalunya, Sept. 2005.

[12] Josep Carmona. “Structural Methods for the Synthesis of Well-Formed Concurrent Specifications”. PhD thesis. Universitat Politècnica de Catalunya, Mar. 2004.

[13] Marco A. Peña. “Relative Timing Based Verification of Concurrent Systems”. Co-advised with Enric Pastor. PhD thesis. Universitat Politècnica de Catalunya, Apr. 2003.

[14] Gianluca Cornetta. “Design and Analysis of Variable-Delay Arithmetic Units”. PhD thesis. Universitat Politècnica de Catalunya, Dec. 2001.

[15] Oriol Roig. “Formal Verification and Testing of Asynchronous Circuits”. PhD thesis. Universitat Politècnica de Catalunya, May 1997.

[16] Enric Musoll. “High-level and logic synthesis techniques for low power”. PhD thesis. Universitat Politècnica de Catalunya, July 1996.

[17] Enric Pastor. “Structural Methods for the Synthesis of Asynchronous Circuits from Signal Transition Graphs”. PhD thesis. Universitat Politècnica de Catalunya, Apr. 1996.

[18] Fermín Sánchez. “Loop pipelining with resource and timing constraints”. PhD thesis. Universitat Politècnica de Catalunya, Jan. 1996.

[19] Rosa M. Badia. “High-level synthesis of asynchronous circuits”. PhD thesis. Universitat Politècnica de Catalunya, July 1994.

[20] Teodor Jové. “Design of instruction memories for pipelined processors”. PhD thesis. Universitat Politècnica de Catalunya, Oct. 1989.

5.2 Master thesis advisor

[1] Víctor Franco. *Combinatorial and Numerical Optimization Techniques for Floorplanning*. Jan. 2024.

[2] Marta Arriaza. *Non-linear models for chip floorplanning*. June 2023.

[3] Pol Barrachina. *AIG transformations to improve LUT mapping in FPGAs*. June 2022.

[4] Júlia Folguera. *Architectural Layout Design with Spectral Methods*. Oct. 2020.

[5] Roberta Priolo. *Proximity-based resource sharing in high level synthesis for FPGAs*. Co-advised with Luciano Lavagno. Dec. 2019.

[6] Narcís Ricart. *Machine learning techniques for resource prediction in nanoelectronic circuit design*. Co-advised with Jonàs Casanova. July 2017.

[7] Alberto Moreno. *Synthesis of timing paths with delays adaptable to integrated circuit variability*. July 2015.

[8] Alexandre Vidal. *SAT-based algorithms for internal cell routing in nanoelectronic circuits*. Co-advised with Jordi Petit. Oct. 2015.

[9] Alex Alvarez. *Library-free technology mapping for VLSI circuits with regular layouts*. Co-advised with Sachin Sapatnekar. July 2014.

[10] Daniel Rivas. *Trace compression mechanisms for the efficient simulation of CMP*. Co-advised with Francesc Guim. July 2014.

[11] Javier de San Pedro. *A simulation framework for hierarchical Network-on-Chip systems*. Co-advised with Josep Carmona. July 2012.

[12] Dmitry Bufistov. *Performance optimization of latency insensitive systems*. Feb. 2008.

[13] Jonàs Casanova. *Clustering for the optimization of asynchronous controllers*. June 2008.

[14] Andrey Ziyatdinov. *Multi-Clustering net Model for VLSI Placement*. Sept. 2008.

[15] Marc Galceran-Oms. *Elastic Esterel*. Co-advised with Gérard Berry. July 2007.

6 Funded research projects

6.1 Grants from Industry

- *Methodology and tools for the specification, synthesis and verification of asynchronous circuits with relative timing*,
  funded by Intel Corporation (Strategic CAD Lab, Hillsboro, OR(USA)), 1999-2002. Principal investigator.
- *Design automation for embedded electronic systems*,
  funded by Cadence Design Systems (Cadence Berkeley Labs, Berkeley, USA), 2001-2003. Principal investigator.
- *Reencoding Techniques for Logic Synthesis of High-speed Circuits*,
  funded by Intel Corporation (Strategic CAD Lab, Hillsboro, OR(USA)), 2002-2004. Principal investigator.
- *Design, synthesis and evaluation of elastic architectures*,
  funded by Intel Corporation (Strategic CAD Lab, Hillsboro, OR(USA)), 2005-2007. Principal investigator.
- *Collaboration agreement between Elastix Corporation and Universitat Politècnica de Catalunya* for research on asynchronous circuits. 2007-2010. Principal investigator.
- *Synthesis of scalable systems for nanoelectronics*,
  funded by Intel Corporation (Strategic CAD Lab, Hillsboro, OR(USA)), 2008-2009. Principal investigator.
- *Floorplanning and performance evaluation for on-die communication fabrics*,
  funded by Intel Corporation (Academic Research Office), 2010-2013. Principal investigator.
- *Cell Synthesis Including Legging, Placement and Routing*,
  funded by Intel Corporation (Strategic CAD Lab, Hillsboro, OR(USA)), 2013. Principal investigator.
- *Macro floorplanning and dataflow automatic analysis for ASICs*,
  funded by eSilicon, 2017. Principal investigator.

6.2 European projects

- *ATD: Technology for ATD* (RACE 1022), 1990–1992. Investigator (principal investigator: Mateo Valero).
- *ACiD-WG: Asynchronous Circuit Design* (ESPRIT-7225), 1992-1995. Principal investigator at UPC.
- *SHIPS: Supercomputer Highly Parallel System* (ESPRIT-6253), 1992-1995. Investigator (principal investigator: Mateo Valero).
- *ACiD-WG: Asynchronous Circuit Design* (ESPRIT-21949), 1996-2000. Principal investigator at UPC.
- *COSY: COdesign, Simulation & sYnthesis* (ESPRIT EP 25443), 1997-2000. Principal investigator at UPC.
- *ACiD-WG: Asynchronous Circuit Design* (IST-1999-21949), 2000-2004. Principal investigator at UPC.
- *SegraVIS: Syntactic and Semantic Integration of Visual Modelling Techniques* (RTN2-2001-00346), 2002-2005. Investigator (principal investigator at UPC: Fernando Orejas).
- *MODERN: MOdeling and DEsign of Reliable, process variation-aware Nanoelectronic devices, circuits and systems* (ENIAC-120003), 2009-2012. Principal investigator as Chief Scientist of Elastic Clocks.

6.3 National projects

- *Design of high-performance low-cost parallel architectures* (CAICYT 314-85), 1986–1989, investigator (principal investigator: Mateo Valero).
- *VLSI architectures oriented to high-level languages* (CICYT TIC80-0300), 1989–1991, principal investigator.
- *Parallel architectures oriented to symbolic applications* (CICYT TIC91-1036), 1991–1994, principal investigator.
- *Design and verification of low-power, high-performance circuits* (CICYT TIC 94-0531-E), 1994–1995, principal investigator.
- *Application-specific high-speed low-power architectures* (CICYT TIC95-419), 1995–1998, principal investigator.
- *Codesign of heterogeneous concurrent systems* (CICYT TIC98-0410), 1999–2001, principal investigator.
- *Heterogeneity and Modularity in the Specification of Systems* (CICYT TIC98-0949), 1999–2001, investigator (principal investigator: Fernando Orejas).
- *Modelling, Analysis and Verification of Heterogeneous Systems* (CICYT TIC2001-2476), 2002-2004, investigator (principal investigator: Fernando Orejas).
- *Graph-based methods for the modelling, analysis and implementation of large-scale systems* (CICYT TIN2004-07925), 2005-2007, investigator (principal investigator: Fernando Orejas).
- *Formal methods and algorithms for system design* (CICYT TIN2007-66523), 2007-2012, investigator (principal investigator: Fernando Orejas).
- *R&D on techniques and CAD tools for the design of asynchronous integrated circuits* (Avanza TSI-020302-2009-20), 2009. Principal investigator as Chief Scientist of Elastic Clocks.
- *Computational models and methods for Massive Structured Data* (TIN2013-46181-C2-1-R), 2014-2017, investigator (principal investigator: Fernando Orejas).

6.4 Integrated actions

- *CAD tools for the synthesis of asynchronous digital circuits*, Integrated action Spain-UK with the University of Newcastle upon Tyne, 1996-97, principal investigator at UPC.
- *Modelling and synthesis of asynchronous arbiters*, Integrated action Spain-Portugal with the University of Aveiro, 1996-97, principal investigator at UPC.
- *CAD tools for the synthesis of asynchronous digital circuits with bounded delays*, Integrated action Spain-UK with the University of Newcastle upon Tyne, 1998-99, principal investigator at UPC.

7 Technology transfer

7.1 Elastix Corporation

In 2007, he co-founded Elastix Corporation, a company aiming at the design of energy-efficient systems using asynchronous design techniques.

7.2 Petrify

`Petrify` is a tool for the synthesis of Petri nets and asynchronous circuits (50,000 lines of C code approximately). The theoretical background of the tool has been a joint work with Dr. M. Kishinevsky (Intel Corp.), A. Kondratyev (Cadence Berkeley Labs), L. Lavagno (Politecnico di Torino), A. Yakovlev (University of Newcastle upon Tyne). This background has been published in numerous journal and conference papers and collected in a book:

> J. Cortadella, M. Kishinevsky, A. Kondratyev, L. Lavagno and A. Yakovlev,
> *Logic Synthesis of Asynchronous Controllers and Interfaces*,
> Springer-Verlag, 2002.

`Petrify` (`http://www.cs.upc.edu/~jordicf/petrify`) is a public domain tool currently being used by more than 20 academic and industrial institutions: Intel Corp., Theseus Logic, Manchester University (UK), Technical University of Denmark, Technion (Israel), AT&T Labs (Cambridge, UK), University of North Carolina at Chapel Hill (USA), etc. `Petrify` ha also been integrated with synthesis flow of Theseus Logic (Sunnyvale, USA) and the logic synthesis system SIS from UC Berkeley.

7.3 Police Criterion Chip

Design and implementation of the *Police Criterion Chip*, an integrated circuit for traffic control in broadband communication network (300.000 transistors, CMOS technology). This prototype was developen within the project RACE 1022 *"Technology for ATD"*. It was a joint work with Anna del Corral and Eduard Elias (from the Computer Architecture Department).

8 Patents

[1] J. Cortadella, L. Lavagno, C. Macián, and F. Martorell. "Asynchronous scheme for clock domain crossing". U.S. pat. 8,433,875. eSilicon Corporation. Apr. 30, 2013.

[2] J. Cortadella, L. Lavagno, and E. Tuncer. "Network of tightly coupled performance monitors for determining the maximum frequency of operation of a semiconductor IC". U.S. pat. 8,446,224. eSilicon Corporation. May 21, 2013.

[3] J. Cortadella, V. Singhal, E. Tuncer, and L. Lavagno. "Variability-aware scheme for high-performance asynchronous circuit voltage regulation". U.S. pat. 8,572,539. eSilicon Corporation. Oct. 29, 2013.

[4] C. Sotiriou, A. Kondratyev, J. Cortadella, and L. Lavagno. "Asynchronous, multi-rail, asymmetric-phase, static digital logic with completion detection and method for designing the same". U.S. pat. 7,870,516. Institute of Computer Science, Foundation for Research and Technology - Hellas. Jan. 11, 2011.

[5] J. Cortadella, V. Singhal, and E. Tuncer. "Variability-aware scheme for asynchronous circuit initialization". U.S. pat. 7,701,255. Elastix Corporation. Apr. 20, 2010.

[6] M. Kishinevsky and J. Cortadella. "Synchronous elastic designs with early evaluation". U.S. pat. 7,657,862. Intel Corporation. Feb. 2, 2010.

[7] J. Cortadella, A. Kondratyev, and L. Lavagno. "Skew insensitive clocking method and apparatus". U.S. pat. 7,634,749. Cadence Design Systems, Inc. Dec. 15, 2009.

9 Academic activities

9.1 Organization and participation in scientific events

Chair and Organizer of events:

- *International Symposium on Advanced Research in Asynchronous Circuits and Systems (ASYNC)*, Member of the Steering Committee.
- *Int. Conf. on Application of Concurrency to System Design (ACSD)*, Member of the Steering Committee.
- *13th Int. Conf. on Application of Concurrency to System Design (ACSD 2013)*, Publicity Chair, Barcelona, July 2013.
- *Design Automation & Test in Europe (DATE)*, Chair of the topic *Logic Synthesis and Timing Analysis*, 2012 and 2013.
- *16th International Symposium on Advanced Research in Asynchronous Circuits and Systems (ASYNC 2010)*, Grenoble, May 2010. Best Paper Chair.
- *14th International Symposium on Advanced Research in Asynchronous Circuits and Systems (ASYNC 2008)*, Newcastle, April 2008. Program co-chair.
- *International Conference on Application and Theory of Petri Nets (ICATPN)*. Program co-chair, 2004.
- *Workshop on Token-Based Computing (ToBaCo)*. Workshop co-organizer, Bologna, June 2004.
- *European Joint Conferences on Theory and Practice of Software (ETAPS)*. Workshop Chair, 2004.
- *Fifth International Symposium on Advanced Research in Asynchronous Circuits and Systems (ASYNC'99)*, Barcelona, April 1999. General chair.
- *Hawaii International Conference on System Sciences*. Hawaii, January 1994. Co-organizer of the mini-track *Design and Prototyping of Digital Signal Processing Systems*.
- *EUROMICRO'93*. Barcelona, September 1993. Conference co-organizer.
- *ACiD-WG Workshop on Digital Signal Processing*. Barcelona, September 1993. Workshop organizer.

Member of Program Committees:

- *Conference on Design, Automation and Test in Europe (DATE)* (1998, 2002, 2006, 2007, 2011–2013).
- *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)* (1997, 1998, 2003, 2014–20162016).
- *ACM/IEEE Design Automation Conference (DAC)* (2007).
- *International Symposium on Advanced Research in Asynchronous Circuits and Systems (ASYNC)* (1996–2000, 2002–2003, 2008–2012, 2014–2016).
- *International Conference on Application and Theory of Petri Nets (ICATPN)* (2001–2003).
- *International Conference on Application of Concurrency to System Design (ACSD)* (1998, 2003).
- *Symposium in Computer Arithmetic* (1997)
- *Joint Conference on Formal Modelling and Analysis of Timed Systems (FORMATS) and Formal Techniques in Real-Time and Fault Tolerant Systems (FTRTFT)* (2004).
- *International Workshop on Formal Modeling and Analysis of Timed Systems (FORMATS)* (2003).
- *Symposium on Integrated Circuits and Systems Design (SBCCI)* (2003).
- *Asian South Pacific Design Automation Conference (ASP-DAC)* (2003).
- *International Symposium on System Synthesis (ISSS)* (2000).
- *IEEE/ACM International Workshop on Logic Synthesis (IWLS)* (1998–2000, 2002, 2003, 2004).
- *Conference in Design of Integrated Circuits and Systems (DCIS)* (1996).
- *Second Working Conference on Asynchronous Design Methodologies* (1995).
- *International Symposium on Microprocessing and Microprogramming* (EUROMICRO) (1990–1994).
- *Conference on Simulation in Electronics* (1994).

Journals and PhD Dissertation Awards:

- Associate Editor of the IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (since Jan 2012).
- Guest Editor of the IEEE Transactions on VLSI Systems Special Section on Asynchronous Circuits and Systems, 2008.
- Member of the evaluation committee of the 2015 ACM SIGDA Outstanding PhD Dissertation Award.
- Reviewer for the following journals:
  - ACM Transactions on Design Automation of Electronic Systems.
  - IEEE Transactions on Computers.
  - IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems.
  - IEEE Transactions on VLSI Systems.
  - IEEE Transactions on Circuits and Systems.
  - IEEE Transactions on Parallel and Distributed Systems.
  - Distributed Computing.
  - Formal Methods in Systems Design.
  - Formal Aspects of Computing: The International Journal of Formal Methods.
  - Fundamenta Informaticae.
  - Integration: The VLSI journal.
  - Journal of VLSI-Signal Processing.
  - IEE Proceedings: Computers and Digital Techniques.
  - Journal on Microprocessing and Microprogramming.

9.2 Positions at the University

9.2.1 Universitat Politècnica de Catalunya

- Member and President of the Commission for the Evaluation and Selection of Academic Staff (CSAPIU), since Nov. 2000 - Dec 2003.
- Member of the Commission of Ph.D. programs, June 1996 - June 2000.

9.2.2 Facultat d'Informàtica de Barcelona (UPC)

- *Vicedean of Resources*, Mar. 1990 - Sept. 1991.
- Member of the Commission for the elaboration of the new Studies Plan, Sept. 1990 - June 1991.

9.2.3 Departament of Computer Science (UPC)

- Head of Department, Feb. 2013 - Jan. 2018.
- Subdirector of Department, Oct 2005 - Dec 2009.
- President of the Comission of Postgraduate Studies, Oct 2005 - June 2007.
- Coordinator of the Ph.D. program in Software, Dec. 1999 - Dec. 2002.

9.2.4 Departament of Computer Architecture (UPC)

- Coordinator of the Ph.D. program in "Computer Architecture and Technology", Apr. 1995 - May 1997.
- Member of the Commission for graduate studies, Oct. 1990 - May. 1994.
- Coordinator of undergraduate studies, Mar. 1989 - Feb. 1990.

10 Publications

10.1 Books and book chapters

[1] Jordi Cortadella. "From Nets to Circuits and from Circuits to Nets". In: *Carl Adam Petri: Ideas, Personality, Impact*. Ed. by Wolfgang Reisig and Grzegorz Rozenberg. Springer, 2019, pp. 227–232. ISBN: 978-3-319-96153-8. DOI: https://doi.org/10.1007/978-3-319-96154-5.

[2] Jordi Cortadella and Sachin S. Sapatnekar. "Static Timing Analysis". In: *Electronic Design Automation for Integrated Circuits Handbook, Second Edition*. Ed. by Luciano Lavagno, Igor L. Markov, Grant E. Martin, and Louis K. Scheffer. CRC Presss, 2016. ISBN: 9781482254501.

[3] Josep Carmona, Jordi Cortadella, Victor Khomenko, and Alex Yakovlev. "Synthesis of Asynchronous Hardware from Petri Nets". In: *Lectures on Concurrency and Petri Nets: Advances in Petri Nets*. Ed. by J. Desel, W. Reisig, and G. Rozenberg. Vol. 3098. Lecture Notes in Computer Science. Springer-Verlag, 2004, pp. 345–401.

[4] Jordi Cortadella and Wolfgang Reisig, eds. *Applications and Theory of Petri Nets 2004*. Vol. 3099. Lecture Notes in Computer Science. Springer-Verlag, 2004.

[5] Josep Carmona, Jordi Cortadella, and Enric Pastor. "Synthesis of Reactive Systems: Application to Asynchronous Circuit Design". In: *Advances in Concurrency and Hardware Design*. Ed. by J. Cortadella, A. Yakovlev, and G. Rozenberg. Vol. 2549. Lecture Notes in Computer Science. Springer-Verlag, 2002, pp. 108–151.

[6] Jordi Cortadella, Michael Kishinevsky, Alex Kondratyev, Luciano Lavagno, and Alexandre Yakovlev. *Logic synthesis of asynchronous controllers and interfaces*. Advanced Microelectronics. Springer-Verlag, 2002.

[7] Jordi Cortadella, Alexandre Yakovlev, and Grzegorz Rozenberg, eds. *Advances in Concurrency and Hardware Design*. Vol. 2549. Lecture Notes in Computer Science. Springer-Verlag, Nov. 2002.

[8] Fermín Sánchez and Jordi Cortadella. "Resource-constrained software pipelining for high-level synthesis of DSP systems". In: *Algorithms and Parallel VLSI Architectures III*. Ed. by M. Moonen and F. Catthoor. Elsevier Science Publishers, 1995.

[9] Jordi Cortadella. "Mechanisms for the efficient execution of branches in RISC architectures". (In Spanish). PhD thesis. Universitat Politècnica de Catalunya, 1987.

[10] Jordi Cortadella, José M. Llabería, and Mateo Valero. "Arquitecturas orientadas a lenguajes basados en la lógica". In: *Inteligencia Artificial*. Ed. Marcombo, 1987. Chap. 21, pp. 233–243.

10.2 Journals

[1] Anna Bernasconi, Valentina Ciriani, Jordi Cortadella, Marco Costa, and Tiziano Villa. "Area-driven Boolean bi-decomposition by function approximation". In: *ACM Transactions on Design Automation of Electronic Systems* 30.1 (Nov. 2024). DOI: 10.1145/3698879.

[2] Lorenzo Lagostina, Filippo Minella, Jordi Cortadella, Mario R. Casu, Mihai T. Lazarescu, and Luciano Lavagno. "Mix & Latch: Comparison With State-of-the-Art Retiming On a RISC-V Benchmark". In: *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* 43.7 (July 2024). DOI: 10.1109/TCAD.2024.3360314.

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11 Tutorials and invited lectures

[1] J. Cortadella. "Extracting Functions from Boolean Relations". Presented at the workshop "*Quo Vadis, Logic Synthesis?*", Design Automation and Test in Europe (DATE), Firenze (Italy). 2019.

[2] J. Cortadella. "Making Petri nets friendlier to engineers". Workshop on Structure Theory of Petri Nets (STRUCTURE 2017), Zaragoza (Spain). 2017.

[3] J. Cortadella. "Adaptive Clocking". Tutorial on Modern Clocking Strategies, presented at the conference *Design Automation and Test in Europe* (DATE). 2016.

[4] J. Cortadella. "Synthesis of asynchronous controllers from Signal Transition Graphs". Lecture at EMICRO/SIM 2016 (18th South Microelectronics School / 31^{st} South Symposium on Microelectronics), Porto Alegre (Brasil). 2016.

[5] J. Cortadella, M. Galceran-Oms, and M. Kishinevsky. "Automatic Pipelining During Sequential Logic Synthesis". EPFL Workshop on Logic Synthesis & Verification. 2015.

[6] J. Cortadella. "Asynchronous circuits". Seminar at the Collège de France within the course on Algorithms, Machines and Languages organized by Gérard Berry. 2013.

[7] J. Cortadella. "Elastic Circuits". Advanced course at EMICRO/SIM 2013 (XV Escola de Microeletrônica Sul / 28^{o} Simpósio Sul de Microeletrônica), Porto Alegre (Brasil). 2013.

[8] J. Cortadella. "Elastic circuits, blending synchronous and asynchronous technologies". Seminar at the Collège de France within the course on Algorithms, Machines and Languages organized by Gérard Berry. 2013.

[9] J. Cortadella, M. Galceran-Oms, and M. Kishinevsky. "Elastic Systems". Invited lecture at the 8th ACM/IEEE International Conference on Formal Methods and Models for Codesign (MEMOCODE), Grenoble (France). July 2010.

[10] J. Cortadella and M. Kishinevsky. "Elasticity and Petri nets". Advanced tutorial at the 28th Int. Conf. on Application and Theory of Petri Nets, Siedlce, Poland. June 2007.

[11] Michael Kishinevsky, Jordi Cortadella, Bill Grundmann, Sava Krstic, and John O'Leary. "Synchronous Elastic Circuits." In: *Computer Science - Theory and Applications, First International Computer Science Symposium in Russia, CSR 2006, St. Petersburg, Russia, June 8-12, 2006, Proceedings*. Ed. by Dima Grigoriev, John Harrison, and Edward A. Hirsch. Vol. 3967. Lecture Notes in Computer Science. Springer, 2006, pp. 3–5.

[12] P.A. Beerel, J. Cortadella, and A. Kondratyev. "Bridging the gap between asynchronous design and designers". Tutorial at the VLSI Design Conference, Mumbai, India. Jan. 2004.

[13] J. Cortadella. "Synthesis of Embedded Software for reactive Systems". Invited lecture at the Int. Workshop on Integration of Specification Techniques for Applications in Engineering (Satellite event of ETAPS 2002). Apr. 2002.

[14] J. Cortadella, M. Kishinevsky, A. Kondratyev, L. Lavagno, and A. Yakovlev. “Hazard free logic synthesis and technology mapping”. Lecture at the Summer School on Asynchronous Circuit Design, (organized by the ACiD-WG, Grenoble). July 2002.

[15] J. Cortadella and A. Yakovlev. “Petrify”. Hands-on tutorial at the Summer School on Asynchronous Circuit Design, (organized by the ACiD-WG, Grenoble). July 2002.

[16] J. Cortadella, A. Yakovlev, and J. Garside. “Logic Design of Asynchronous Circuits”. Tutorial at the ASP-DAC/VLSI Design Conference, Bangalore, India. Jan. 2002.

[17] J. Cortadella. “Tools for automatic synthesis and verification of asynchronous interfaces”. Invited lecture at the workshop “Asynchronous Interfaces: Tools, techniques, and implementations” (AINT’2000), Delft, The Netherlands. July 2000.

[18] J. Cortadella, M. Kishinevsky, A. Kondratyev, and L. Lavagno. “Introduction to asynchronous circuit design: specification and synthesis”. Tutorial at the 6th Int. Symp. on Advanced Research in Asynchronous Circuits and Systems, Eilat, Israel. Apr. 2000.

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[20] Jordi Cortadella, Michael Kishinevsky, Alex Kondratyev, Luciano Lavagno, and Alexandre Yakovlev. “Hardware and Petri nets: Application to asynchronous circuit design”. Invited lecture at the 21st Int. Conf. on Application and Theory of Petri Nets, Aarhus, Denmark. June 2000.

[21] J. Cortadella. “STG-based synthesis and Petrify”. Tutorial at the 3rd ACiD-WG Workshop, Newcastle upon Tyne, UK. Jan. 1999.

[22] J. Cortadella. “Asynchronous circuit verification and synthesis with Petri nets”. Invited lecture at the Workshop on Hardware Design and Petri Nets , Lisbon. June 1998.

[23] J. Cortadella. “Combining structural and symbolic methods for the verification of concurrent systems”. Invited lecture at the International Conference on Application of Concurrency to System Design (CSD’98), Aizu-Wakamatsu, Japan. Mar. 1998.

[24] M. Kishinevsky, J. Cortadella, and A. Kondratyev. “Asynchronous Interface Specification, Analysis and Synthesis”. Embedded tutorial at the Design Automation Conference, San Francisco, USA. June 1998.

[25] J. Cortadella and M. Kishinevsky. “Synthesis of control circuits from STG specifications”. Course in the Summer School on Asynchronous Circuit Design (organized by the ACiD-WG, ESPRIT 21949), Lyngby, Denmark. Aug. 1997.

[26] J. Cortadella, E. Macii, G. De Micheli, M. Pedram, J. Rabaey, and K. van Berkel. “What’s Hot in Low Power Design ?” Participation at the panel session at the European Design Automation Conference (EURO-DAC), Geneve, Switzerland. Sept. 1996.

[27] J. Cortadella. “Executing Branch Instructions with Zero Time Delay in a RISC”. Invited lecture at the IEEE Computer Society Workshop on VLSI, Clearwater Beach, USA. Feb. 1988.

[28] J. Cortadella. “Arquitecturas RISC”. Invited lecture at the IV Jornadas de Diseño Lógico, Barcelona. 1987.