Bibliography

Asynchronous WWW pages and bibliography

Here are some links to the *Asynchronous Logic Homepage* and *Bibliography*.

[Gar] Jim Garside. The Asynchronous Logic Homepage. `http://www.cs.man.ac.uk/amulet/async/`.

[Peea] Ad Peeters. The 'Asynchronous' Bibliography Homepage. http://www.win.tue.nl/async-bib/async.html.

[Peeb] Ad Peeters. The 'Asynchronous' Bibliography (BibTeX) database file `async.bib`. http://www.win.tue.nl/async-bib/doc/async.bib. Corresponding e-mail address: `async-bib@win.tue.nl`.

Books

Here are some relevant books for asynchronous design. The book [SF01] is an introductory text on asynchronous design. The book [CKK+02] covers the part on logic synthesis from concurrent specifications. The other books are complementary for different subjects on design, synthesis and verification of asynchronous circuits.

[Ber93] Kees van Berkel. *Handshake Circuits: an Asynchronous Architecture for VLSI Programming*, volume 5 of *International Series on Parallel Computation*. Cambridge University Press, 1993.

[BS95] Janusz A. Brzozowski and Carl-Johan H. Seger. *Asynchronous Circuits*. Springer-Verlag, 1995.

[CKK+02] J. Cortadella, M. Kishinevsky, A. Kondratyev, L. Lavagno, and A. Yakovlev. *Logic Synthesis of Asynchronous Controllers and Interfaces*. Springer-Verlag, 2002.

[KKTV94] Michael Kishinevsky, Alex Kondratyev, Alexander Taubin, and Victor Varshavsky. *Concurrent Hardware: The Theory and Practice of Self-Timed Design*. Series in Parallel Computing. John Wiley & Sons, 1994.

[Mye01] Chris Myers. *Asynchronous Circuit Design*. John Wiley & Sons, 2001.

[SF01] Jens Sparsø and Steve Furber, editors. *Principles of Asynchronous Circuit Design: A Systems Perspective*. Kluwer Academic Publishers, 2001.

Seminal papers and special issues

[BJN99] C. H. (Kees) van Berkel, Mark B. Josephs, and Steven M. Nowick. Scanning the technology: Applications of asynchronous circuits. *Proceedings of the IEEE*, 87(2):223–233, February 1999.

[Cha84] Daniel M. Chapiro. *Globally-Asynchronous Locally-Synchronous Systems*. PhD thesis, Stanford University, October 1984.

[CM74] Wesley A. Clark and Charles E. Molnar. Macromodular computer systems. In Ralph W. Stacy and Bruce D. Waxman, editors, *Computers in Biomedical Research*, volume IV, chapter 3, pages 45–85. Academic Press, 1974.

[Fur95] S. Furber. Computing without clocks: Micropipelining the ARM processor. In Graham Birtwistle and Al Davis, editors, *Asynchronous Digital Circuit Design*, Workshops in Computing, pages 211–262. Springer-Verlag, 1995.

[Mar86] Alain J. Martin. Compiling communicating processes into delay-insensitive VLSI circuits. *Distributed Computing*, 1(4):226–234, 1986.

[MB59] David E. Muller and W. S. Bartky. A theory of asynchronous circuits. In *Proceedings of an International Symposium on the Theory of Switching*, pages 204–243. Harvard University Press, April 1959.

[MLM+97] Alain J. Martin, Andrew Lines, Rajit Manohar, Mika Nyström, Paul Pénzes, Robert Southworth, and Uri Cummings. The design of an asynchronous MIPS R3000 microprocessor. In *Advanced Research in VLSI*, pages 164–181, September 1997.

[Sei80] Charles L. Seitz. System timing. In Carver A. Mead and Lynn A. Conway, editors, *Introduction to VLSI Systems*, chapter 7. Addison-Wesley, 1980.

[Sut89] Ivan E. Sutherland. Micropipelines. *Communications of the ACM*, 32(6):720–738, June 1989.

[Ung69] S. H. Unger. *Asynchronous Sequential Switching Circuits.* Wiley-Interscience, John Wiley & Sons, Inc., New York, 1969.

Complementary bibliography used in the tutorial

[ABZV03] Aseem Agarwal, David Blaauw, Vladimir Zolotov, and Sarma Vrudhula. Statistical timing analysis using bounds. In *Proc. Design, Automation and Test in Europe (DATE)*, pages 10062–10067, March 2003.

[CG03] Ajanta Chakraborty and Mark R. Greenstreet. Efficient self-timed interfaces for crossing clock domains. In *Proc. International Symposium on Advanced Research in Asynchronous Circuits and Systems*, May 2003.

[CKLS03] Jordi Cortadella, Alex Kondratyev, Luciano Lavagno, and Chirstos Sotiriou. A concurrent model for de-synchronization. In *Proc. International Workshop on Logic Synthesis*, June 2003.

[CN01] Tiberiu Chelcea and Steven M. Nowick. Robust interfaces for mixed-timing systems with application to latency-insensitive protocols. In *Proc. ACM/IEEE Design Automation Conference*, June 2001.

[Cum03] Uri Cummings. Removing design bottlenecks with switch-based system interconnects. In *Archives of the 2003 Communications Design Conference*, October 2003.

[Gre95] Mark R. Greenstreet. Implementing a STARI chip. In *Proc. International Conf. Computer Design (ICCD)*, pages 38–43. IEEE Computer Society Press, 1995.

[KL02] Alex Kondratyev and Kelvin Lwin. Design of asynchronous circuits by synchronous cad tools. In *Proc. ACM/IEEE Design Automation Conference*, pages 411–414, June 2002.

[Lin03] Andrew Lines. Nexus: an asynchronous crossbar interconnect for synchronous system-on-chip designs. In *Proceedings of the 11th Symposium on High Performance Interconnects*, pages 2–9, August 2003.

[Nas01] S.R Nassif. Modeling and analysis of manufacturing variations. In *Proc. of Asia and South Pacific Design Automation Conference*, May 2001.

[OB02] Recep O. Ozdag and Peter A. Beerel. High-speed QDI asynchronous pipelines. In *Proc. International Symposium on Advanced Research in Asynchronous Circuits and Systems*, pages 13–22, April 2002.

[YD99] Kenneth Y. Yun and A. E. Dooply. Pausible clocking-based heterogeneous systems. *IEEE Transactions on VLSI Systems*, 7(4):482–488, December 1999.