Increasing the Robustness of Digital Circuits with Ring Oscillator Clocks

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***Abstract*—Technology scaling enables lower supply voltages, but also increases power density of integrated circuits. In this context, power integrity becomes a major concern in the implementation of high-performance designs. This paper analyzes the influence of Ring Oscillator Clocks (ROCs) on mitigating the impacts of voltage noise. A design with an ROC as the clock source is able to work correctly even in the presence of severe and unpredictable voltage emergencies, without degrading the average performance and power metrics of the circuit. ROCs offer an instantaneous and continuous adaptation to the environment conditions, thus reducing the guardband margins used to prevent timing failures. ROCs provide robustness independently of the parameters of the power delivery network, thus relaxing the constraints required for the design of the PCB and package. As a by-product, the inherent jitter generated by ROCs produces a spread-spectrum effect that reduces electromagnetic emissions.**

I. INTRODUCTION

A key factor for the reliability of digital circuits is the correct estimation of the path delays and their variability [1]. In order to define a robust clock period for a synchronous design, it is necessary to consider all conditions that may shift and affect the delay of every path in the circuit, such as the supply voltage, the temperature and the manufacturing process. Static offsets of the operating conditions are predicted at design time and taken into account by adding guardband margins to the nominal clock period. Nevertheless, dynamic shifts are hard to predict and excessively conservative timing margins are often added to prevent failures.

Augmenting the clock period offers more robustness against changes in the operating conditions, but unfortunately this comes at the expense of reducing performance or increasing power. Another simple and expensive solution is to increase the amount of decoupling capacitors (decaps) [2], [3]. Voltage noise is mitigated when the system has a larger on-chip and off-chip capacitance. Unfortunately, variations that exceed the defined margins cannot be fully eliminated. Considering the use of embedded systems with integrated circuits in safety critical applications, this is a risk that must be mitigated.

Another approach to cope with unforeseen variations is the use of resilient circuits with error detection techniques [4], which allow timing errors to happen and then recover the circuit to a correct state. This method may be useful and eficient for some applications, but it has high complexity and overhead. Adaptive clocking [5], [6] is a promising solution to deal with a wider range of operating conditions. However, this approach depends on the characteristics of the sensors for voltage, temperature and aging [7], and may not always react correctly to unpredicted events such as large voltage droops.

Ring Oscillator Clocks [8], [9] are an alternative clock source paradigm, which *adapt* the clock period *instantaneously* to the delay of the critical paths. ROCs can be considered an adaptive clocking proposal, which takes into account all sources of variability, with low complexity and low overhead. Notice that the ROC and the critical paths are exposed to the same sources of variability. Therefore, if the ROC is correctly designed for a circuit, then a strong correlation is obtained between the clock period and the delays of the critical paths.

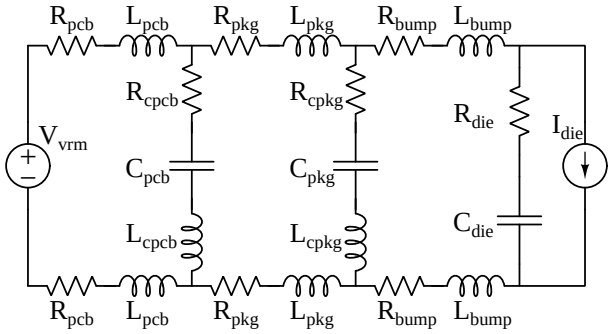


Fig. 1. PDN model.

This work attempts to demonstrate that ROCs are a *natural solution* to work robustly in the presence of voltage variations. Experiments using an actual design and PDN are performed to illustrate the advantages of ROCs even in the presence of large voltage swings.

The design decision of using an ROC instead of a Phase-Locked Loop (PLL) as the clock source introduces a series of benefits that are presented in this paper:

- **Robustness during voltage swings**: ROCs react *instantaneously* to voltage fluctuations and adapt the clock period to the delay of the critical paths, as it will be discussed in Sect. III. Consequently, it is possible to reduce timing margins while having a robuster circuit.
- **Independence of PDN parasitics**: the clock period of an ROC always adapts to the voltage of the circuit, regardless of the characteristics of the PDN. As discussed in Sect. IV, the same design can work correctly for different PDNs without degrading average performance when using an ROC.
- **Electromagnetic Interference (EMI) mitigation**: several works in the literature [10]–[12] propose the *insertion of jitter* in the clock source, in order to obtain a more spreaded frequency spectrum of the clock and reduce EMI. ROCs have high clock jitter and contribute to mitigate EMI, as evidenced in Sect. V.

II. BACKGROUND

A. Voltage droops

The PDN is responsible for distributing the power and ground voltages to all devices of the design and is usually constituted by the following components: voltage regulator (VRM), board (PCB), package (PKG), connection bumps, and on-chip power distribution network [3]. These components have parasitic inductances, resistances and capacitances, which can be modeled as depicted in Fig. 1. Decaps are usually placed at all levels of the PDN in order to reduce voltage fluctuations. These capacitances have parasitics as well, which are also known as equivalent series inductance (ESL) and equivalent series resistance (ESR). The inductances and capacitances interact with each other, forming LC circuits with different resonance frequencies, which are responsible for the *voltage droops*.

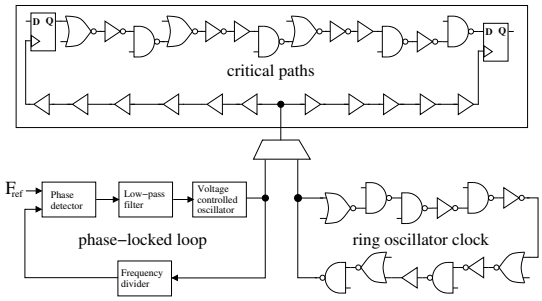


Fig. 2. Synchronous circuit with a PLL or an ROC as the clock source.

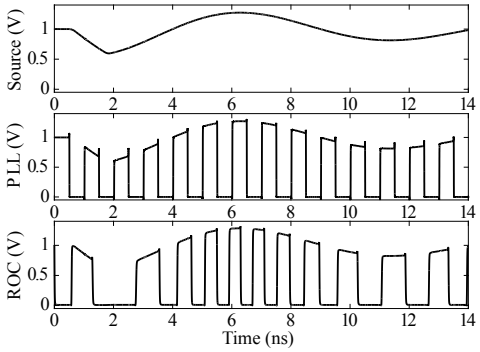


Fig. 3. PLL and ROC clock generation in the presence of voltage noise.

The circuit composed by $C_{\rm die}$ and $L_{\rm bump}$ generates the *first droop*, which typically has the largest voltage noise amplitude and a resonance frequency of 100-400MHz [13]. The second and third droops usually have lower resonance frequencies and amplitudes compared with the first droop. The second droop is controlled by $C_{\rm pkg}$ and $L_{\rm pkg}$, and the third droop is dominated by $C_{\rm pcb}$ and $L_{\rm pcb}$. Note that the first droop is the closest to the chip, the severest and directly affects the design performance.

For designers, it is difficult to anticipate whether voltage emergencies will actually show up in their designs. Very often, they just *conjecture* that these events will not happen, without a full guarantee of safety. Note that the same circuit designed for an application can be used for other purposes, with changes in the operating frequency, the submodules activated, the firmware, and the packaging. In this context, it is very difficult to predict the presence of such large voltage fluctuations. Still, if a voltage emergency occurs, then a timing failure may be originated and the circuit operation becomes impredictable.

B. Ring oscillator clocks

Jitter and other clock uncertainties are typically covered by increasing the timing margins of the clock period, degrading circuit performance. For that reason, the use of ROCs as clock source has been discarded, as they have a high jitter caused by their sensitivity to the various sources of variability.

Figure 2 shows a synchronous circuit fed by a PLL or by an ROC, depending on the selection of a multiplexer. Figure 3 illustrates the clock signals generated by the PLL and the ROC when a voltage droop occurs. The clock period of the PLL is not affected by the changes in the voltage source, as it is designed to support variations and deliver a low-jitter clock. However, the circuit paths have a different behavior: their delay increases when voltage decreases.

When the PLL is selected as the clock source, timing failures are avoided by adding margins that consider the delay of the critical paths at the *minimum estimated voltage*. On the other hand, the period of the ROC is modified by the voltage variation, as seen in Fig. 3.

TABLE I
PDN PARAMETERS.

Parameter	Value	Parameter	Value
R_{pcb}	0.094 mΩ	R_{cpkg}	0.54 mΩ
L_{pcb}	21 pH	L_{cpkg}	5.61 pH
R_{cpcb}	0.17 mΩ	C_{pkg}	26 μF
L_{cpcb}	1 pH	R_{bump}	0.3 mΩ
C_{pcb}	240 μF	L_{bump}	0.5 pH
R_{pkg}	1 mΩ	R_{die}	0.0025 mΩ
L_{pkg}	120 pH	C_{die}	400 nF

Recent studies [8], [9] demonstrate that the jitter of ROCs is highly correlated with the delay variability of the circuit paths. In other words, the PVT variations suffered by the ROC are perceived by the circuit paths in an analogous way, as they are composed of similar logic gates. For example, when the circuit path becomes slower due to a voltage droop or a temperature increase, the frequency of the ROC slows down as well. This correlation between the jitter of ROCs and the circuit delay variations enables the reduction of timing margins, and hence improve circuit performance or reduce power [8], [9].

Obviously, it does not exist an exact match between the delay of the critical paths and the period of an ROC. First of all, standard cells have different responses to PVT variations. Additionally, there are voltage and temperature differences across the chip, and process variability is not identical throughout the die [14]. Moreover, unknown or not well-understood issues must be covered, such as aging and radiation. Notwithstanding, the most significant variations are strongly correlated between the critical paths and the ROC, as demonstrated in Sect. III-B.

In this work the conventional clock source (PLL) is replaced by an ROC, that is implemented according to the guidelines described in [8]. In summary, the design process of an ROC consists of:

- Delay extraction of the critical paths of the circuit.
- Use the delay data to create a similar path using library gates.
- Organize these gates in a ring to generate an oscillating signal.

The delay extraction is performed for all PVT corners available in the technology, using STA tools (Synopsys Primetime® in this work). The extracted delays are the input to a path synthesizer tool, which produces a single chain of standard cells that is able to produce an oscillating signal, i.e. a clock. Note that the design of an ROC depends only on the manufacturing technology and the variability behavior. Hence, it is agnostic to the characteristics of the chip or the package.

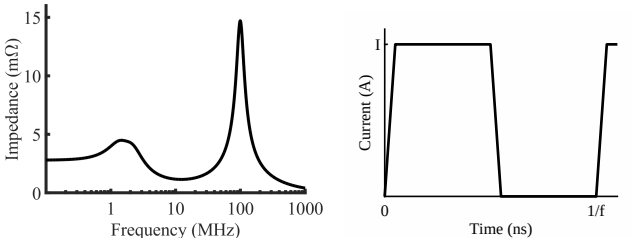
III. Robustness during voltage swings

A circuit is able to work correctly under *virtually any* voltage droop with the aid of an ROC. This section presents the setup used for the experiments in the paper, and demonstrates the timing robustness of ROCs during voltage emergencies.

A. Experimental setup

All experiments are performed through simulations using the tool Synopsys HSPICE®. The PDN shown in Fig. 1 is described in a SPICE netlist using the values of Table I, which are in concordance with state-of-the-art literature [13], [15], [16]. Figure 4(a) shows the impedance response of the PDN modeled. The first and second droops are located at 100MHz and 2MHz, respectively, with the impedance at the first droop more than 3× larger than at second droop. The third droop is masked by the second droop.

The design used as reference comprises 10 instances of an AES [17] encryption module organized in a 5×2 matrix, all operating in the same clock and power domain. This design is synthesized, placed and routed using the tools Synopsys Design Compiler® and



(a) Impedance response (b) Current source waveform

Fig. 4. Chip-package impedance response and current source waveform.

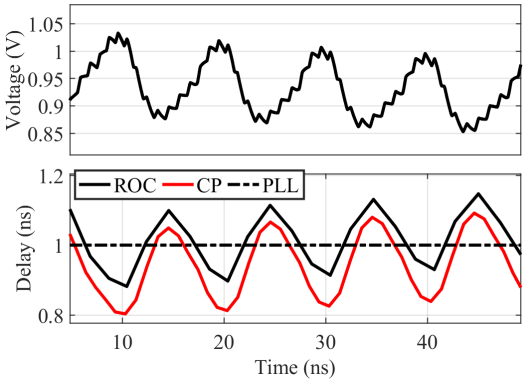


Fig. 5. Voltage droops and its effects on the delay of the critical paths and the period of the ROC and the PLL.

Synopsys IC Compiler®. The standard cell library is provided by the foundry, using a 65nm commercial technology with a nominal voltage of 1V. The target operating frequency is 1GHz, achieving a timing margin (slack) of 154ps at 1V and 125°C. An ROC designed to operate at 1GHz is implemented using gates of the library and represented by a SPICE netlist. The main critical paths of the circuit are also described in a SPICE netlist.

The reference circuit is modeled using a resistor, a capacitor and a current source [3], as depicted in Fig. 1. The resistor and the capacitor values are extracted and scaled accordingly to model a design with similar size as the ones presented in [16], [18]. The template waveform of the current source emulating the circuit operation is shown on Fig. 4(b), with rise, high and fall times set to 5%, 60%, and 5%, respectively. The amplitude and frequency of the current source vary for each experiment. For any case, the current amplitude is adjusted to the voltage variations, as they are correlated.

It is assumed that the critical paths and the ROC have the same voltage at a time. This assumption is valid for small circuits, as the one analyzed herein. For larger circuits, the small voltage differences across the die can be handled by OCV margins used in conventional sign-off procedures, or by increasing the amount of ROC domains, reducing the voltage difference between the ROC and the critical paths. Still, large voltage droops have a dominant global component that affects all the chip similarly [19].

B. Slack in the presence of voltage emergencies

This section demonstrates that slack is always positive when an ROC is used as the clock source, even in the presence of large voltage swings. In contrast, timing is easily violated for the same scenario with a PLL, degrading performance in order to support such fluctuations in the supply voltage.

In this experiment, the current amplitude is set to 39A at operating frequency (1GHz) to emulate the operation of the circuit.

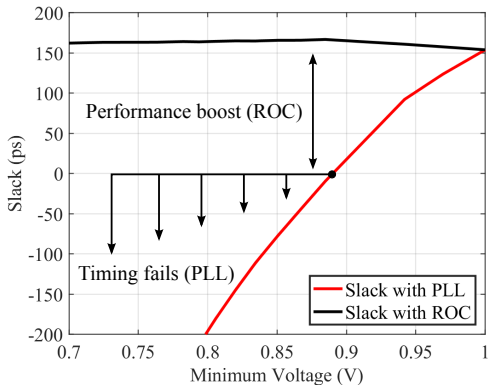


Fig. 6. Slack analysis for PLL and ROC.

Additionally, a current source of 15.6A is set at first droop frequency (100MHz) in order to stimulate voltage droops. Figure 5 illustrates the large variations in the supply voltage generated by this setup, and the resulting effects on the delay of the critical paths (CP) and the period of the PLL and the ROC.

As observed in Fig. 5, the PLL period is fixed and it is not affected by the voltage fluctuations, while the delay of the critical paths varies instantaneously with the voltage. Notice that timing is violated when the voltage is lower than 0.89V, which is a typical 10% variation estimated in a multi-corner STA sign-off.

Figure 5 also depicts the evolution of the ROC with the same design and for the same time window and setup. In this case, the clock period also fluctuates with the voltage and its variations are similar to the ones of the critical paths delay. Thus, ROCs do not eliminate voltage emergencies, but enable the circuit to work correctly when these phenomena happen. Moreover, timing robustness is achieved without degrading performance, as the average period of the ROC is the same as the PLL.

Figure 6 shows the time slack of the same design for a larger range of voltage levels, using the PLL and the ROC. For the PLL, negative slacks appear when voltage drops below 0.89V. For the ROC, the slack remains almost constant regardless of the voltage droop severity. A minor slack difference is observed across different voltages because the delay response of the ROC and the critical paths is not exactly the same, as the sensitivity of each standard cell to voltage variations is different. The slack may be larger for lower voltages if the cells in the ROC have a larger threshold voltage than the ones in the critical paths, for example.

The plot in Fig. 6 does not only illustrate the extreme robustness to voltage variations, but also the capability of improving performance (or reducing power) by narrowing the margins required to cover variability. For instance, in this example it is possible to boost average performance by 15% with no issues for timing closure, simply by switching the clock source from the PLL to the ROC.

IV. Independence of PDN Characteristics

Voltage emergencies occur rarely, and the resonant frequency at which these events take place depends on the PDN. The design of the PDN is an arduous task that must take into account the target frequency of the chip, the PDN parasitics and decaps. It is necessary to adjust the characteristics of the PDN in order to avoid undesired voltage droops, which may happen when the switching activity is aligned with some resonance frequency of the PDN.

This section shows how the robustness of ROCs contributes to *relax* the constraints for the design of the PDN, given the tolerance

TABLE II
PARAMETERS OF THE PDNS.

	R_{cpkg}	L_{cpkg}	Resonance Freq.	Peak Impedance
PDN 1	0.54 mΩ	5.61 pH	100 MHz	15 mΩ
PDN 2	0 mΩ	0 pH	253 MHz	4 mΩ
PDN 3	n/a	n/a	16 MHz	220 mΩ

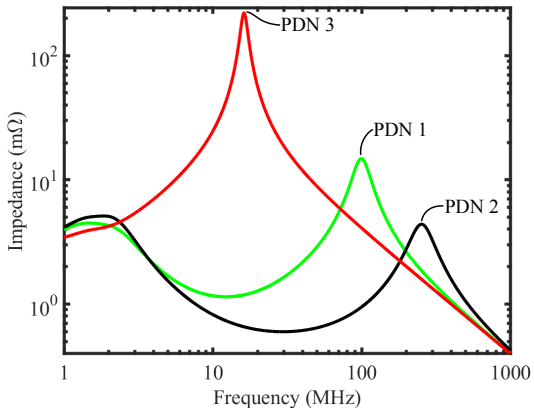


Fig. 7. Impedance responses of the PDNs analyzed.

to handle voltage emergencies. For this purpose, an analysis with different PDN parameters for the same design is performed, under the worst-case assumption that there is a periodical current difference aligned with the resonant frequency of the PDN. Three different PDNs have been constructed (parameters shown in Table I):

- PDN 1: the one used in Sect. III, which models a PDN with a flip chip (low inductance L_{bump}).
- PDN 2: ideal package decaps (without ESL and ESR), maximizing voltage noise mitigation.
- PDN 3: without package decaps, increasing the equivalent inductance that forms the LC circuit with C_{die}.

Figure 7 depicts the impedance response for each of the PDNs described. It is observed that PDN 2 has the lowest impedance at the first droop and voltage noise is significantly mitigated by the absence of parasitics in the package decaps. Although unrealistic, the impedance response of PDN 2 evinces the high quality of the PDN used in the experiment of Sect. III.

On the opposite side, the removal of package decaps increases the equivalent resistance and inductance connected to the chip and results in a very high impedance at the first droop. In practice, PDN 3 has a similar impedance response at the first-droop region as if the flip chip interconnection would be replaced by a wire bonding, which has larger inductance and resistance.

In order to enforce voltage emergencies for all PDNs and compare their impact on the reference performance, a current source of 28A was generated and aligned with the first-droop frequency[1]. This current is large enough for provoking a voltage emergency in the best PDN (-114mV for PDN 2) and not invading the sub-threshold region for the worst PDN (PDN 3).

Figure 8 shows the maximum reliable frequency for the PLL and the ROC average frequency. For the PLL, it is necessary to cover the deepest droops and ensure that the delay of the critical paths are always shorter than the clock period. A PDN with a larger impedance response produces larger voltage droops. The largest generated droops were -200mV, -114mV and -515mV for each PDN, respectively, leading to a performance degradation of up to 90% for PDN 3.

[1]First-droop frequency is different for each PDN, as described in Table I.

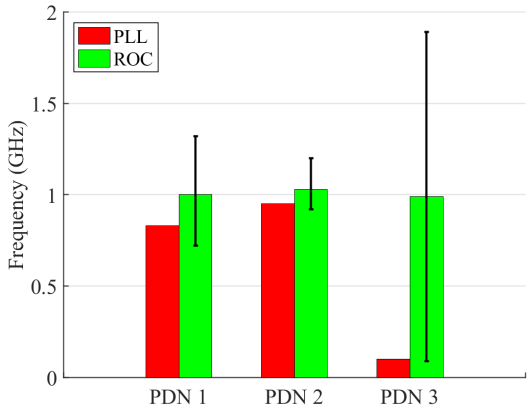


Fig. 8. PLL and ROC performance with the different PDNs.

The vertical lines for ROC in Fig. 8 represent the range of frequencies observed during the simulations, corresponding to the maximum overshoot and minimum undershoot of the supply voltage. Notice that the minimum ROC frequency is lower than the PLL frequency. The reason is that the ROC is more sensitive to voltage droops and its delay scales slightly different from the one of the critical paths, thus safely increasing the guardband slack. However, the average frequency of the ROC is always larger, as expected.

Several important conclusions can be drawn from this experiment:

- Voltage droops have a very important impact in performance when using rigid clock schemes. For this reason, a significant effort must be invested in designing high-quality PDNs. This phenomenon is shown for PDN 3 (in an unrealistic scenario, but illustrative enough to demonstrate how harmful a low-quality PDN can be).
- ROCs can *surf* over deep voltage fluctuations. Therefore, low-quality PDNs can accommodate circuits with ROCs without degrading performance.
- The average frequency of the circuit is almost independent from the characteristics of the PDN, as shown in Fig. 8.
- Systems operating with ROCs must tolerate frequency variations along the executing time of the applications. However, an average frequency can be sustained. This frequency can be larger than the one required for a PLL [8], [9].

V. ELECTROMAGNETIC INTERFERENCE MITIGATION

Electromagnetic interference (EMI) is an aspect that must be considered to comply with the regulations in the application domain. In digital systems, EMI is mostly produced by the periodic current differences around clock edges. For this reason, most of the energy is concentrated around certain harmonics of the clock frequency.

Several techniques are typically used to mitigate electromagnetic radiations. Shielding is often used to isolate the product from the external world, but this technique has a significant cost [11]. A less costly approach is the use of spread-spectrum clock generators (SSCG), that outspread the energy over a wider bandwidth and reduce peak amplitude [10]–[12]. This technique consists of adding intentional jitter to the clock generator, which implies additional timing margins.

In this work, it was demonstrated that the period of an ROC depends directly on the voltage. The presence of high currents produces voltage fluctuations that, at the same time, implicitly injects jitter to the clock period. Fortunately, this jitter does not need to be margined since the period variability is highly correlated with

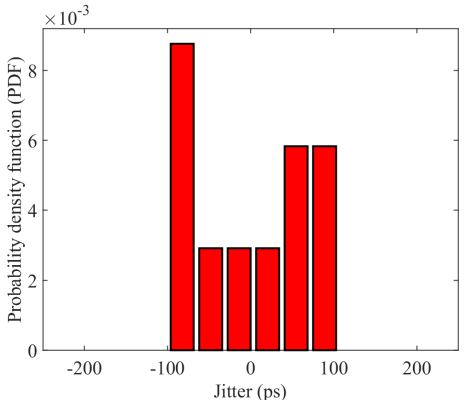


Fig. 9. ROC jitter probability distribution.

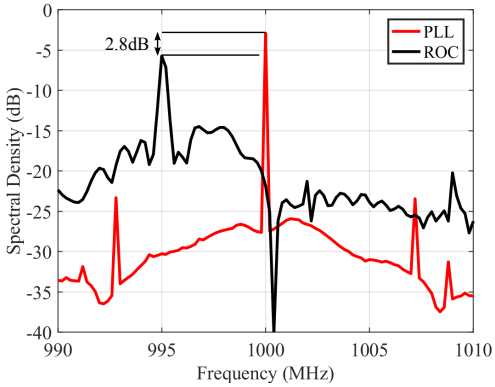


Fig. 10. Frequency spectrum comparison of ROC vs. PLL.

the circuit delays. Therefore, a *natural* spread-spectrum effect is produced without degrading performance.

In order to analyze the clock jitter of ROCs and the EMI reduction, an experiments has been performed by generating a current profile identical to the experiment in Sect. III-B. Notice that this current profile is periodic, with a fixed amplitude. The ROC is calibrated to have an average clock frequency of 1 GHz, the same as the PLL. Results are obtained by SPICE simulations along $10\mu s$.

The histogram in Fig. 9 illustrates the period jitter probability at each clock cycle, with respect to the ROC average period. ROC probability density function is larger at lower and higher jitter values as result of voltage undershoots and overshoots, respectively.

The frequency spectrum of the ROC and the PLL are compared in Fig. 10. As expected, the jitter introduced by the ROC produces a spread spectrum effect, reducing the peak amplitude in 2.8dB. For comparison, [12] reports a 13dB peak reduction for a $\pm 3\%$ spread in their SSCG design, which implies a 3% performance degradation. We have to bear in mind that the design of an ROC is much simpler than the one of a SSCG.

It is important to mention that the results obtained in this work are not measured, but simulated. Also, the only source of variability analyzed is the supply voltage, in a very simple and periodic current profile. Therefore, the results shown in this section indicate that the EMI reduction can be larger for real designs using ROCs, with both the current randomness and the variability increased. Furthermore, any EMI reduction produced by an ROC comes *for free*, i.e., does not degrade performance and does not require any explicit mechanism to address EMI.

VI. Conclusions

Power integrity is major design concern nowadays due to the low supply voltages and power density in high-performance circuits. ROCs have been shown to be a competitive alternative to the classical rigid clocks generated by PLLs.

ROCs do not only provide significant advantages in performance and/or power, but a robust scheme to tolerate unpredictable fluctuations in power supply voltages and live with low-quality PDNs. EMI mitigation is another by-product of this adaptive clocking scheme.

We are facing a future in which many devices will have to operate in environments with scarce energy in which scavenging mechanisms will be essential. Providing reliable DC voltages under these scenarios may be difficult and costly. ROCs emerge as a potential solution to operate robustly in hostile environments with low-cost PDNs. Furthermore, considering the use of integrated circuits in safety critical applications, the ROCs characteristic of adaptating to undesirable operating conditions may be crucial to support situations of scarce energy or large voltage noise.

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