Design for testability using mixed-polarity flip-flops and latches

Lorenzo Lagostina*, Jordi Cortadella†, Mario R. Casu*, Luciano Lavagno*
*Department of Electronics and Telecommunications, Politecnico di Torino, Torino, Italy
†Department of Computer Science, Universitat Politècnica de Catalunya, Barcelona, Spain
Emails: lorenzo.lagostina@polito.it, jordi.cortadella@upc.edu, mario.casu@polito.it, luciano.lavagno@polito.it

***Abstract*—Sequential circuits employing a combination of mixed-polarity flip-flops and latches allow significant improvements in clock frequency compared to useful skew and retiming. However, no work addresses the task of enabling a scan- based test on a circuit optimized with such techniques, while simultaneously minimizing the area overhead due to shadow latches used to complete the scan chain when latches are used in the design. This poses a serious limitation to the industrial application of mixed FF and latch-based techniques, since post-fabrication tests are an unavoidable step in IC production. This paper presents a macro-cell structure to enable both the exploitation of time borrowing for frequency optimization and the execution of the scan test of a design. The proposed solution requires minimal changes in the test setup and is evaluated using a recent methodology, *Mix&Latch*. Moreover, the work proposes modifications to *Mix&Latch* that allow reusing the standard cells introduced for the scan test to solve hold timing violations, avoiding additional hardware overhead. Results show that the lumped cell structure does not significantly impact frequency gains, and the ILP formulation of latch and FF type optimization can be extended to cover the DFT optimization part, ensuring only a moderate increase in area and power consumption, comparable with the DFT impact on regular FF-based designs.**

***Index Terms*—Design for testability, latch-based circuit, digital IC, scan test, latches**

I. Introduction

Latches can deliver a wide range of benefits when used in digital circuits, ranging from frequency improvement [1]–[3], power consumption reduction [4], and enabling error-resilient applications [5]. Moreover, using both polarities for latches and FFs (i.e., positive and negative edge FFs and positive and negative level latches) increases the clock frequency beyond what is achievable with retiming and useful skew [6]. The literature on Design-For-Testability (DFT) [7], while already covering the testing of latch-based designs [8], presents a gap regarding the scan chain test in designs employing latches and flip-flops active on both polarities using commercial tools. This is crucial for the adoption of this type of technique in the industry, as compliance with Electronic Design Automation (EDA) tools is mandatory for fabricating Application Specific Integrated Circuits (ASICs). To address this problem, we propose a methodology that consists of:

1) Synthesizing an FF-based design, creating the scan chain and a specific test setup which will be discussed in a later section;
2) Running the Automatic Test Pattern Generation (ATPG) on the FF-based netlist;
3) Modifying the circuit by substituting setup-critical scan FFs with a macro-cell that allows exploiting latch time-borrowing while maintaining the scan chain for testing. In this paper we assume, for ease of discussion, that all registers are implemented with scan FFs. The methodology can be extended directly to partial scan.
4) To test the effectiveness of our proposal, we use a recent methodology, *Mix&Latch* [6], to automatically apply our structure to an FF-based netlist.

The technique mentioned above substitutes regular flip-flops with Positive Transparent Latches (PTLs) to increase the maximum achievable frequency through latch time-borrowing, and then solves an Integer-Linear Programming (ILP) model to fix the eventual hold violations using Negative Transparent Latches (NTLs) as retention barriers. We propose modifications to this algorithm that allow reusing some of the hardware of the scan chain to fix these hold violations.

Our main contributions to the state-of-the-art are the following:

1) Proposal of a macro-cell structure to attain both latch time borrowing and scan chain test.
2) Definition of guidelines that allow using commercial EDA tools for DFT and facilitate the industrial application of mixed-polarity FFs and latches.
3) A set of changes of the ILP-based optimization of *Mix&Latch* to exploit NTLs in the scan chain to fix hold violations, while minimizing sequential area.
4) Experiments on three different circuits from the ISCAS89 [9] and CEP [10] benchmarks that demonstrate that the proposed structure provides very similar clock frequency gains through time borrowing, with limited area and power overhead, to what was achieved by the original authors of [6], where DFT was not considered.

II. Related Work

A. Alternatives to PETF-based circuits

The literature presents several techniques that explore alternatives to purely Positive-Edge-Triggered-Flops(PETF)-based digital circuits. An example is the pulsed latch design [2], [11]–[13], which exploits narrow high clock pulses to achieve a timing behavior similar to that of the sampling of FFs in a latch-based design, with the benefit of reduced area and power from the latch cells. This comes at the cost of additional

978-3-9826741-1-7/DATE26/© 2026 EDAA
Authorized licensed use limited to: UNIVERSITAT POLITECNICA DE CATALUNYA. Downloaded on July 29,2026 at 07:39:56 UTC from IEEE Xplore. Restrictions apply.

hardware to generate clock pulses for each sequential block and the difficulty of distributing these narrow pulses reliably.

Other works use two different clock phases in cases such as solving timing violations for sub-threshold circuits [4], and latch-based implementation of Razor logic [5]. The authors of [3] propose using three clock phases for a latch-based design to reduce area occupation and power consumption, but with a more difficult clock-tree layout problem.

Works that adopt solutions based on a single clock phase include [14], which proposes to split PETFs into couples of latches, and retiming the resulting PTLs using commercial tools. In [6], [15], [16], the authors present solutions to transform FF-based designs into latch-based or mixed designs.

B. Testing in latch-based and mixed designs

The authors of [17] propose a method to test a mixed circuit based on both latches and FFs using two clock phases, while we rely on the more standard single-clock approach. The work in [18] focuses on testing pipelines composed of alternating stages of NTLs and PTLs, while we address arbitrary mixes of FFs and latches.

Although it focuses on FF-based design, [19] is an interesting work that proposes a different implementation of the master latch inside the FFs to improve reliability during the scan test.

III. Scan Latch Structure

A. A deconstruction of the Scan Flip-Flop to create scan latches

Similarly to [14], where a FF is split in its two latches, our proposal starts by looking at the structure of a scan FF, namely a multiplexer and an FF, with the latter composed of an NTL and a PTL. The purpose of our work is to understand whether it is possible to have a structure that keeps the original scan chain structure while also allowing to exploit latch time borrowing. Our solution is to move the NTL in the middle of the structure before the multiplexer, on the path of the Scan-In, removing from the scan FF the setup constraint of the clock edge, resulting in the schematic in Fig. 1. This structure is somewhat similar to that used in Level Sensitive Scan Design (LSSD) [20], in which, instead of using a scan FF, additional logic is inserted to force scan values on the master latch (NTL) of the flop to scan.

The most straightforward way to implement this ”Scan Latch” structure is to use standard cells already provided by technology libraries and lump them together into a macro-cell to be used by DFT directly. The realization of the full layout of a dedicated standard cell is not the scope of this study and is left for future work. Given the excellent results that we obtain, it does not promise significant gains.

B. Adapting commercial DFT to use scan latches

Commercial EDA tools tend to provide limited support for latch-based designs. Hence the scan latch structure that we propose requires a set of specific guidelines to ensure compatibility with some such tools (in particular, those from Synopsys satisfy our requirements). Since there is currently no support for the insertion of PTL registers (not to be confused with the lockup

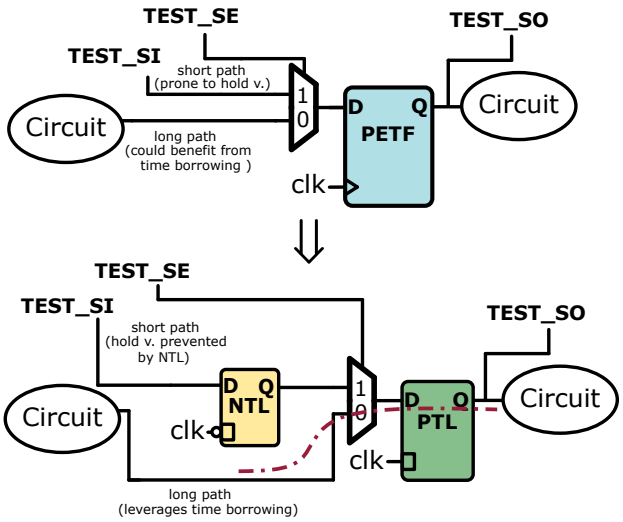

Fig. 1. Proposed scan latch structure. The NTL on the Scan-In path allows sampling test patterns during the scan phase, while allowing time borrowing in functional mode.

latches used to solve hold violations in regular FF-based scan chains [21]) in commercial DFT tools, we introduce the scan FF discussed above after logic synthesis and the creation of the scan chain, which we perform with Synopsys Design Compiler, as shown in Fig. 2. Henceforth we indicate with ⓐ-ⓔ the edges of Fig. 2. After the synthesis and substitution of FFs, we also define the test clock, whose high phase must not be wider than that of the active phase of the functional clock. This is necessary to ensure that hold constraints are not violated during the test phase. Note that the high phase width can be reduced due to the lower frequency of the test clock. Then we generate the directives for the ATPG ⓐ (in our case, Tetramax from Synopsys), to generate test patterns and the testbench to simulate the scan chain. In this work we use ATPG to cover stuck-at-faults. Finally, we modify the circuit by substituting a subset of scan FFs, identified with any method that uses latches to improve timing, such as [6], with the scan latch circuit discussed in Section III-A. In this step it is necessary to update the testbench ⓓ, annotating the new Scan-In points of the registers. Logic simulations using Synopsys VCS showed no loss in scan test functionality.

C. Evaluating time borrowing effectiveness using Mix&Latch

Having verified that performing a scan test with the proposed structure is possible, we still have to check whether it is possible to exploit time borrowing, or if the added hardware poses a limitation to frequency gains. To perform this evaluation we need to observe the behavior of a circuit with this structure not only during RTL synthesis, but also during physical synthesis (P&R), implementing different Register Transfer Level (RTL) designs, i.e. (1) with and without DFT and (2) with and without mixed-polarity FF and latch usage. A recent methodology that exploits the latter, called *Mix&Latch* [6], appeared to be compatible with our proposal, and by reaching out to the authors,

Authorized licensed use limited to: UNIVERSITAT POLITECNICA DE CATALUNYA. Downloaded on July 29,2026 at 07:39:56 UTC from IEEE Xplore. Restrictions apply.

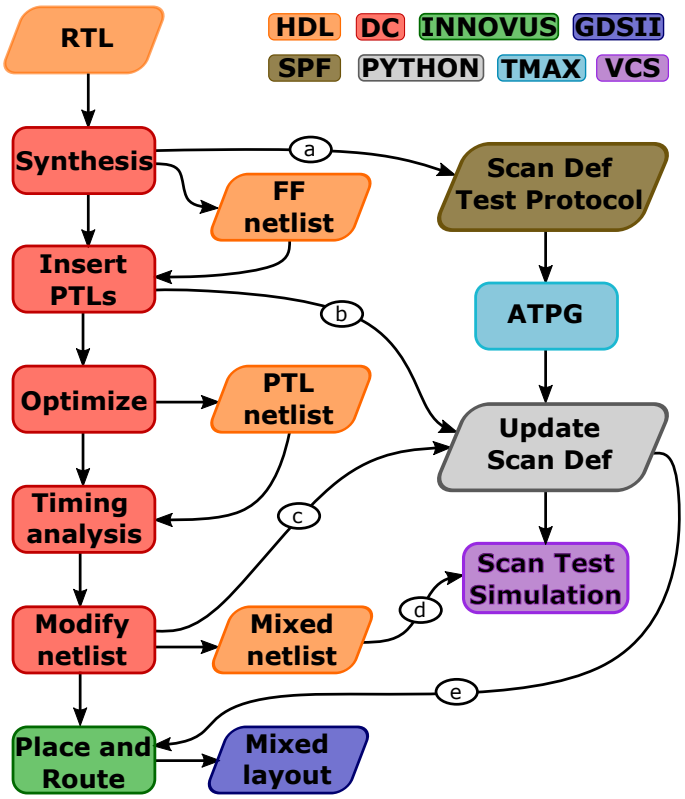

Fig. 2. *Mix&Latch* flow (left) and proposed passages for DFT implementation (right). Numbers highlight the connection point between the two flows. Colors indicate if the type of files, and the tool/language used,

we managed to get access to their algorithm implementation to perform our experiments.

1) Mix&Latch methodology: The *Mix&Latch* technique, displayed in Fig. 2 with modifications to integrate our proposal, works as follows:

1) At the end of logic synthesis, part or all of the FFs are substituted with PTLs. This relaxes setup constraints due to latch time borrowing, at the cost of tighter hold constraints.
2) Create a graph with timing information about the hold-violated paths.
3) Use the graph to formulate an ILP problem, that once solved provides a set of locations in the circuit to insert NTLs. These NTLs delay signals on short paths by half a clock cycle, fixing hold violations.
4) The cost function of the ILP is formulated to minimize the number of sequential elements in the final circuit In particular, if an NTL is placed immediately before or after a PTL, they are merged together in a Positive-Edge-Triggered-Flop (PETF), or a Negative-Edge-Triggered-Flop (NETF), respectively. Additionally, constraints to the ILP ensure that the delay introduced by NTLs does not cause setup violations.

2) Modifications to optimize sequential area when using DFT: In this paper, in addition to the scan-based strategy discussed in III-A, we propose a variation of the *Mix&Latch* ILP formulation that simultaneously (1) fixes the hold violations caused by the presence of PTLs and (2) minimizes the area of sequential elements while considering the impact of DFT requirements discussed in Section III-B. Note that, since we aim to increase the clock frequency of the design in functional mode, scan chain paths are not analyzed when applying the *Mix&Latch* methodology. The only requirement discussed above for the scan mode is that the high phase of the test clock cannot be wider than that of the functional clock. The analysis requires examining the various configurations of FFs and latches after NTL insertion by *Mix&Latch*.

In Fig. 3 we show the case in which an NTL is to be placed before the multiplexer input corresponding to the data pin of the scan latch discussed above. This means that the PTL was not necessary to improve the achievable clock frequency (because an NTL followed by a PTL is just a PETF), and the resulting structure can be replaced by a regular scan FF cell. Thus the ILP solutions that cause this type of insertion of an NTL have a lower weight than those that insert an NTL far from a PTL, which would require additional shadow latches for scanning.

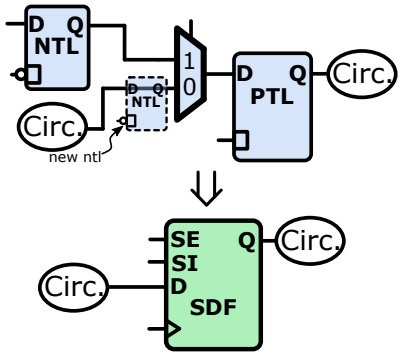

Fig. 3. Instead of adding an NTL in front of the 0 input of the multiplexer, in parallel to the scan NTL, the cells highlighted in blue are merged into a Scan FF.

The other two cases that allow the reuse of scan latch cells are those in which an NTL is placed after a scan FF or latch, along the path that leads to the combinational logic, and where a scan latch is present further downstream in the scan chain. In the first case, shown in Fig. 4, we use the subsequent NTL, introduced to enable scanning the PTL to the right, to also solve the hold violation without introducing additional hardware. Thus the cost of this solution is favored in the ILP cost function.

Similarly, in the case displayed in Fig. 5, we connect the combinational logic input to the scan NTL of the following stage, and merge the resulting MUX-PTL-NTL structure into a scan NETF, removing two sequential elements. This is also favored by the new ILP cost function proposed in this paper.

3) Performing Placement and Routing: Once the ILP problem is solved and the netlist is modified as discussed above, we implement the physical layout of the design (in this paper we use Cadence Innovus, but the methodology is not tool-specific). Note that, while the tool can automatically recognize the scan chain when implemented with scan FFs and lockup latches along the chain, it fails to do so when unexpected cells, such

Authorized licensed use limited to: UNIVERSITAT POLITECNICA DE CATALUNYA. Downloaded on July 29,2026 at 07:39:56 UTC from IEEE Xplore. Restrictions apply.

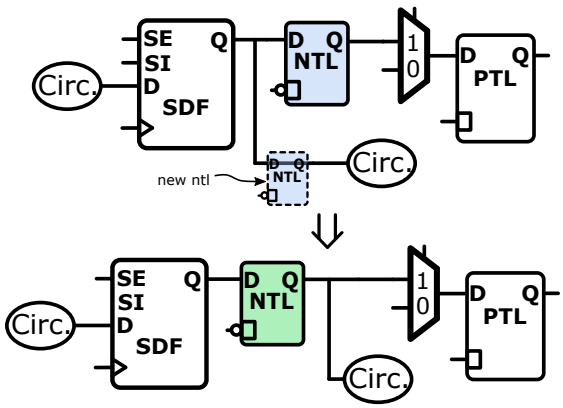

Fig. 4. The highlighted NTL, introduced for scanning, is used to solve the hold violation, connecting the logic circuit to the NTL's output instead of the Scan PETF.

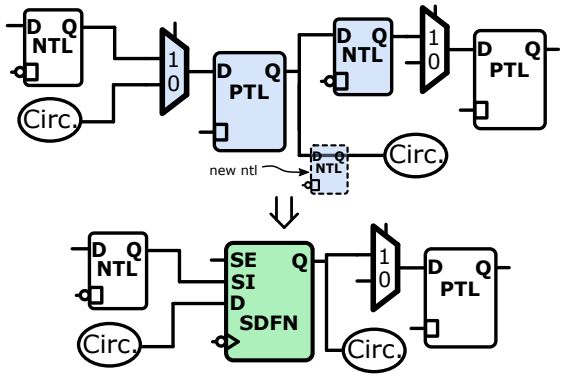

Fig. 5. In addition to the modification of Fig 4, here the highlighted cells are merged in a scan NETF.

as MUXes, are used, and registers are not implemented using FFs. To address this issue, we generate a DEF file with the description of the FF-based scan chain before applying the scan latches, and annotate all the modifications to the netlist ⓑⓒ to ultimately update the scan chain definition using a Python script. Finally, the DEF file can be used during P&R ⓔ.

IV. Experimental Setup

To evaluate the effects of our approach in terms of Performance, Power and Area, we start by finding the maximum clock frequency for which timing constraints are satisfied at the end of P&R, using only PETFs both for the DFT and no DFT cases (baseline); using a $28\,\mathrm{nm}$ technology library. Then we apply our modified DFT-aware version and the original *Mix&Latch* respectively, by sweeping the target clock frequency from the best achieved with PETFs to $+50\,\%$ higher. For each clock period, following the *Mix&Latch* approach [22], we use different configurations parameters, namely:

- Change the percentage of FFs substituted with PTLs (or scan latches), ranging from those with setup slack at their input lower than $0\,\%$ of the clock (i.e., exactly those on the the setup-critical paths), up to those with setup slack lower than $100\,\%$ of the clock period (i.e. all the FFs) with a $5\,\%$ step, which enables exploring different area/performance trade-offs.
- Relax/tighten hold and/or setup constraints, ranging from $-10\,\%$ to $+20\,\%$ of the clock period with a $5\,\%$ step.

V. Results

We ran experiments for three different circuits, `s15850`, from the ISCAC89 benchmark, `sha256` and `aes192`, both from the CEP benchmark. The `s15850` circuit has a few thousands of logic elements, the `sha256` almost $10\,\mathrm{k}$, and the `aes192` almost $200\,\mathrm{k}$. Fig. 6, Fig. 7, and Fig. 8 report the results in terms of area versus target frequency after the P&R step, for both the cases in which DFT is applied and not applied. The left-most points in these plots are the baseline points, i.e. the maximum frequency points of the regular FF-based implementation. Points with a light blue border identify the designs where DFT is applied. The figures also show for each point the solutions chosen by the ILP solver, divided in:

- Merging two latches in one FF (no DFT case);
- Insertion of an additional NTL (both cases);
- Movement of an existing NTL (DFT case);
- Merging of three elements in a scan FF (DFT case).

As we can observe in Fig. 6, for the `s15850` design, the no DFT approach (lower sequence of points, without light blue border) is better than the one with DFT (upper sequence of points, with light blue border) in terms of both area occupation and maximum frequency achieved. This design is the smallest of the three and sequential cells occupy almost half of the total area, while for the other two the sequential area is closer to one quarter of the total. In the two larger circuits, however, the maximum achieved frequency is the same with and without DFT, and the DFT solution has a lower area overhead compared to the no DFT version.

This result is counterintuitive, as we expect DFT to decrease the maximum frequency and increase the final area, as shown by the two baseline points. To better understand this behavior, we can analyze the choices made by the ILP solver during the experiments. This shows that in the DFT case the most common solution is to merge back different elements in a scan flip-flop (light green), while in the no DFT cases the insertion of additional NTLs (orange) is chosen more often, also becoming the dominant solution at the highest frequency points of the `aes192` design. We also observed a positive correlation between the number of sequential elements (reported in Table I) and the final area. This supports the hypothesis that *merging sequential elements in the circuit is the proximate cause of the area difference*.

Looking for the root cause of this difference, we further analyzed the timing metrics after the first substitution of FFs with the PTLs or the scan latch macro respectively. Static Timing Analysis shows that the implementations resulting in higher area present more hold violations (hundreds to thousands of violations in the no DFT case, tens in the DFT case), which are also more severe (hundreds of picoseconds against 10s in the DFT case). Additionally, the documentation of the $28\,\mathrm{nm}$ technology library used in the experiments shows that

Authorized licensed use limited to: UNIVERSITAT POLITECNICA DE CATALUNYA. Downloaded on July 29,2026 at 07:39:56 UTC from IEEE Xplore. Restrictions apply.

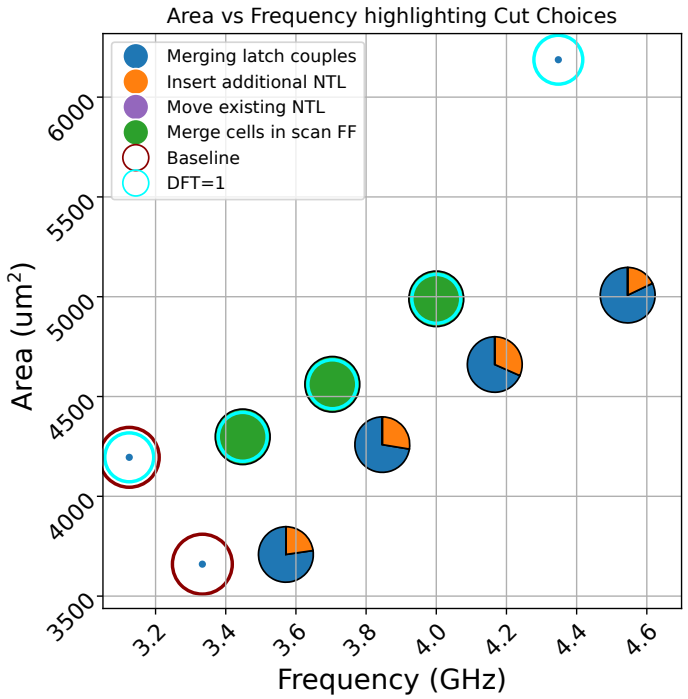

Fig. 6. Area occupation versus target frequency and ILP solutions for the `s15850` design.

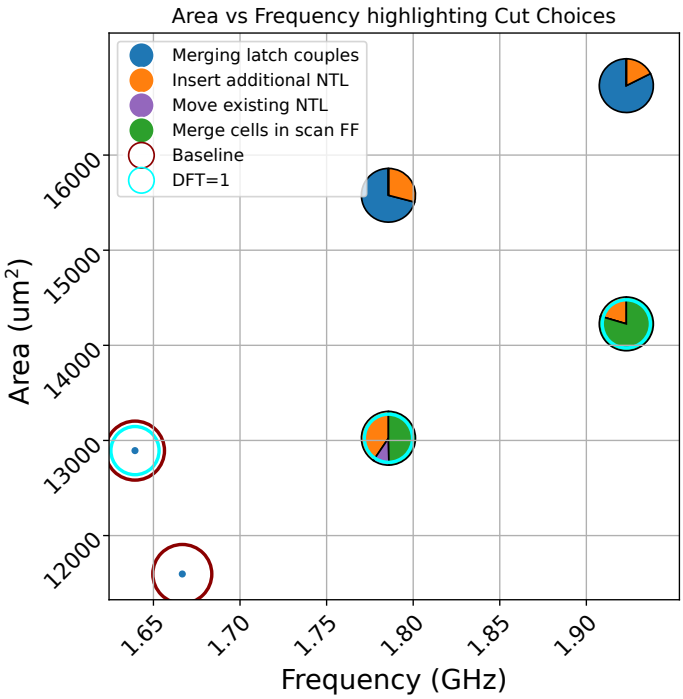

Fig. 7. Area occupation versus target frequency and ILP solutions for the `sha256` design.

for PETFs without scan functionality there are only 5 different cell sizes available, whilst for the same kind of PETF with scan functionality there are 19, possibly because the library is optimized for industrial designs, where full scan dominates. Our hypotheses to explain this behavior are:

- The multiplexer added with the macro-cell introduces a delay that, although small (about 20 ps), reduces the severity of hold violations, removing the smallest ones;
- The difference in terms of available PETF cells can lead to different optimization choices by Design Compiler when the additional compilation is performed after the FF substitution.

We can thus conclude that using our scan latch macro allows us to reach similar frequency improvements as using the *Mix&Latch* methodology without DFT, without introducing significant area overhead.

Concerning power consumption, it is statically estimated from Innovus and results are reported in Table I. Power follows the same trend as area, with increased consumption in the same no DFT cases that show the area overhead. Therefore, we also conclude that our proposal does not introduce significant increases in terms of power consumption.

VI. Conclusions and Future Work

This article introduces a macro-cell that allows time borrowing in a circuit while attaining the scan test functionality of a scan FF. We then use a recent methodology called *Mix&Latch* to evaluate the impact in terms of PPA when combining time borrowing with scan. Moreover, we propose modifications to the *Mix&Latch* formulation to effectively reuse the hardware introduced with our scan latch structure to solve the hold violations caused by the use of PTLs in the circuit. We perform synthesis, DFT insertion, ATPG and Place&Route using commercial tools and a 28 nm technology library. Results show how the proposal achieves similar results in terms of maximum achieved frequency compared to the original *Mix&Latch* flow, without incurring in significant overheads in terms of area and power. Future work will concentrate on creating a physical layout of a standard cell to implement the functionalities of our scan latch macro.

References

[1] B. Taskin and I. Kourtev, "Time borrowing and clock skew scheduling effects on multi-phase level-sensitive circuits," in *2004 IEEE International Symposium on Circuits and Systems (IEEE Cat. No.04CH37512)*, vol. 2, 2004, pp. II–617.

[2] Y. Shin and S. Paik, "Pulsed-Latch Circuits: A New Dimension in ASIC Design," *IEEE Design Test of Computers*, vol. 28, no. 6, pp. 50–57, 2011.

[3] H. Cheng, X. Li, Y. Gu, and P. A. Beerel, "Converting Flip-Flop to Clock-Gated 3-Phase Latch-Based Designs using Graph-Based Retiming," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, pp. 1–1, 2021.

[4] M. Pons, T.-C. Le, C. Arm, D. Séverac, J.-L. Nagel, M. Morgan, and S. Emery, "Sub-threshold latch-based icyflex2 32-bit processor with wide supply range operation," in *2016 46th European Solid-State Device Research Conference (ESSDERC)*, 2016, pp. 33–36.

[5] M. Fojtik, D. Fick, Y. Kim, N. Pinckney, D. M. Harris, D. Blaauw, and D. Sylvester, "Bubble Razor: Eliminating Timing Margins in an ARM Cortex-M3 Processor in 45 nm CMOS Using Architecturally Independent Error Detection and Correction," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 1, pp. 66–81, 2013.

[6] F. Minnella, J. Cortadella, M. R. Casu, M. T. Lazarescu, and L. Lavagno, "Mix & Latch: An Optimization Flow for High-Performance Designs With Single-Clock Mixed-Polarity Latches and Flip-Flops," *IEEE Access*, vol. 11, pp. 35 830–35 840, 2023.

Authorized licensed use limited to: UNIVERSITAT POLITECNICA DE CATALUNYA. Downloaded on July 29,2026 at 07:39:56 UTC from IEEE Xplore. Restrictions apply.

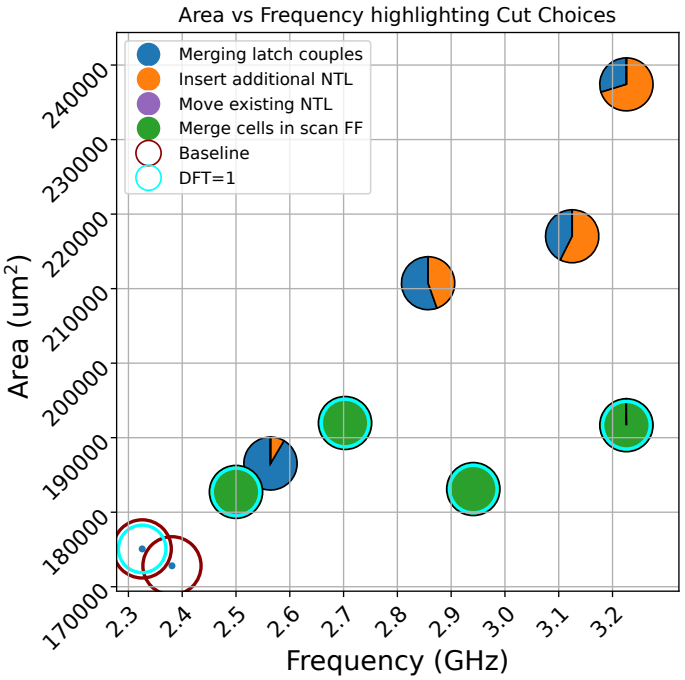

Fig. 8. Area occupation versus target frequency and ILP solutions for the `aes192` design.

TABLE I

PPA METRICS FOR EACH BENCHMARK CIRCUIT, SHOWING AREA, NUMBER OF SEQUENTIAL ELEMENTS, AREA OF SEQUENTIAL ELEMENTS, AND POWER CONSUMPTION, HIGHLIGHTING IF THE FLOW ONLY EMPLOYED FF REGISTERS (FF), OR IF IT RELIES ON A MIXED COMBINATION OF LATCHES AND FLOP WITH MIXED POLARITY (MIX), AND IF DFT IS USED.

s15850						
Flow	DFT	Freq. (GHz)	Area (μm^2)	#Seq. Cells	Seq. Area (μm^2)	Power (mW)
FF	N	3.33	3660.05	571	1760.98	17.38
Mix	N	3.57	3708.6	816	2025.07	18.03
Mix	N	3.85	4258.97	833	2236.58	22.27
Mix	N	4.17	4660.32	830	2463.55	27.75
Mix	N	4.55	5007.74	766	2507.57	30.97
FF	Y	3.13	4195.23	591	2337.55	19.77
Mix	Y	3.45	4298.11	794	2062.54	18.84
Mix	Y	3.70	4561.37	822	2099.66	20.68
Mix	Y	4.0	4989.43	851	2224.49	23.64
Mix	Y	4.35	6187.44	1182	2363.26	26.34
sha256						
Flow	DFT	Freq. (GHz)	Area (μm^2)	#Seq. Cells	Seq. Area (μm^2)	Power (mW)
FF	N	1.67	11596.2	1298	3947.83	37.06
Mix	N	1.79	15577.3	1549	4504.25	55.23
Mix	N	1.92	16729.8	1575	4688.71	63.73
FF	Y	1.64	12893.16	1298	4833.86	40.16
Mix	Y	1.79	13023.02	1509	5000.02	40.47
Mix	Y	1.92	14225.57	1494	5138.95	50.4
aes192						
Flow	DFT	Freq. (GHz)	Area (μm^2)	#Seq. Cells	Seq. Area (μm^2)	Power (mW)
FF	N	2.38	172809.84	9505	33869.30	310.32
Mix	N	2.56	186530.74	10401	39182.64	390.49
Mix	N	2.86	210726.94	14364	50952.22	522.28
Mix	N	3.13	217027.272	16338	52290.0	575.89
Mix	N	3.23	237406.34	21809	55995.74	585.18
FF	Y	2.33	175077.17	9511	37610.33	289.05
Mix	Y	2.5	182724.53	9587	42657.89	341.11
Mix	Y	2.7	191969.57	9562	47752.15	407.23
Mix	Y	2.94	183107.23	12661	40505.64	381.8
Mix	Y	3.23	191674.73	12697	43276.3	446.84

[7] H. Fujiwara, *Logic testing and design for testability*. MIT press Cambridge, MA, 1985.

[8] K. Y. Chung and S. K. Gupta, "Design and test of latch-based circuits to maximize performance, yield, and delay test quality," in *2010 IEEE International Test Conference*. IEEE, 2010, pp. 1–10.

[9] F. Brglez, D. Bryan, and K. Kozminski, "Combinational profiles of sequential benchmark circuits," in *Circuits and Systems, 1989., IEEE International Symposium on*, May 1989, pp. 1929–1934 vol.3.

[10] MIT-LL, "Common Evaluation Platform (CEP)," https://github.com/mit-ll/CEP.git, 2021.

[11] J.-F. Lin, "Low-Power Pulse-Triggered Flip-Flop Design Based on a Signal Feed-Through," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 22, no. 1, pp. 181–185, 2014.

[12] H. Lee, S. Paik, and Y. Shin, "Pulse Width Allocation and Clock Skew Scheduling: Optimizing Sequential Circuits Based on Pulsed Latches," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 29, no. 3, pp. 355–366, 2010.

[13] S. Paik, L.-e. Yu, and Y. Shin, "Statistical time borrowing for pulsed-latch circuit designs," in *2010 15th Asia and South Pacific Design Automation Conference (ASP-DAC)*, 2010, pp. 675–680.

[14] K. Yoshikawa, K. Kanamaru, S. Inui, Y. Hagihara, Y. Nakamura, and T. Yoshimura, "Timing optimization by replacing flip-flops to latches," in *ASP-DAC 2004: Asia and South Pacific Design Automation Conference 2004 (IEEE Cat. No.04EX753)*, 2004, pp. 186–191.

[15] K. Singh, H. Jiao, J. Huisken, H. Fatemi, and J. P. de Gyvez, "Low power latch based design with smart retiming," in *2018 19th International Symposium on Quality Electronic Design (ISQED)*, 2018, pp. 329–334.

[16] N. A. N. Hassan, A. B. Abd Manaf, and L. C. Ming, "Optimization of circuitry for power and area efficiency by using combination between latch and register," in *2011 IEEE International Conference on Computer Applications and Industrial Electronics (ICCAIE)*, 2011, pp. 240–244.

[17] U. Shpiro, K. Wee, K.-H. Tsai, J. Zawada, and X. Lin, "Test challenges of intel ia cores," in *2020 IEEE International Test Conference (ITC)*. IEEE, 2020, pp. 1–5.

[18] K. Y. Chung and S. K. Gupta, "Design and test of latch-based circuits to maximize performance, yield, and delay test quality," in *2010 IEEE International Test Conference*. IEEE, 2010, pp. 1–10.

[19] R. Ma, S. Holst, X. Wen, A. Yan, and H. Xu, "Stahl: A novel scan-test-aware hardened latch design," in *2019 IEEE European Test Symposium (ETS)*. IEEE, 2019, pp. 1–6.

[20] E. B. Eichelberger and T. W. Williams, "A logic design structure for lsi testability," in *Papers on Twenty-Five Years of Electronic Design Automation*, ser. 25 years of DAC. New York, NY, USA: Association for Computing Machinery, 1988, p. 358–364. [Online]. Available: https://doi.org/10.1145/62882.62924

[21] V. R. Rani and M. Samson, "Enhancing dft performance: The power of scan compression and lockup latches," in *2024 4th International Conference on Ubiquitous Computing and Intelligent Information Systems (ICUIS)*, 2024, pp. 1835–1841.

[22] L. Lagostina, F. Minnella, J. Cortadella, M. R. Casu, M. T. Lazarescu, and L. Lavagno, "Mix & latch: Comparison with state-of-the-art retiming on a risc-v benchmark," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 43, no. 7, pp. 2229–2233, 2024.

Authorized licensed use limited to: UNIVERSITAT POLITECNICA DE CATALUNYA. Downloaded on July 29,2026 at 07:39:56 UTC from IEEE Xplore. Restrictions apply.