Synthesis of Speed-Independent Circuits from STG-unfolding Segment

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Abstract
This paper presents a novel technique for synthesis of speed-independent circuits. It is based on partial order representation of the state graph called STG-unfolding segment. The new method uses approximation technique to speed up the synthesis process. The method is illustrated on the basic implementation architecture.

Introduction
The problem of synthesis of speed-independent circuits from their Signal Transition Graph (STG) specifications has been approached by many researchers. Several tools exist today, such as SIS [10], Assassin [12], Forcage [3] and Petrify [2], which are capable of synthesising circuits of moderate size. All but Forcage use some form of State Graph (SG) representation to obtain truth tables of the implementation logic. Petrify uses Binary Decision Diagrams (BDDs) to represent SG symbolically and can thus synthesise circuits from larger descriptions. Forcage, on the other hand, uses Change Diagrams (partial order model) to derive an implementation but is restricted to specifications without choice.

Construction of SG hits available computational limits due to state explosion. A structural method in [6] can implement STGs avoiding exhaustive state exploration. It uses concurrency relation between transitions of the STG to obtain an initial approximation of the implementation. If this approximation does not satisfy correctness criteria, the refinement process is performed using SM Machine (SM) decompositions. Although powerful, this method is restricted to SM-decomposable specifications.

The main goal of this work is to develop a method for implementing STGs that cannot be synthesised by the above techniques due to the large size of their SG. A way to achieve this goal will be analogous to the one in [6] – it will draw upon relations at the event-based, rather than state-based, description level. This method will, however, be free from the limitations of [6].

The solution to this problem is found in the use of a partial order approach, already known to have given positive results in STG verification. It is based on an implicit representation of SG in the form of a finite STG-unfolding segment [9]. It was shown [9] that such a segment can often be built for those examples where the construction of SG fails. While the segment is being constructed it is also verified for correctness. Thus, after the verification stage is completed, an implementation can be derived from an already built STG-unfolding segment. Two approaches are possible within the new synthesis method: exact and approximate. The former obtains an implementation equivalent to that derived from the SG. At the end of the synthesis procedure this approach produces an implementation by recovering binary states from the segment (similar to the approach of [5]). Although it benefits from the unfolding methodology which restricts the set of states needed to examine for each signal, the exact approach may suffer from exponential explosion of states. To battle the complexity, the latter approach uses concurrency relation to initially approximate and then to refine an approximated implementation. The structural method of [6] works on the STG level, assuming that two transitions are concurrent if they can ever fire simultaneously. Loose approximation may require several computationally costly refinement iterations. On the contrary, our method works with a partial run of the STG specified behaviour. Thus it is possible to pin-point when exactly any two transitions become concurrent. This local information gives a more accurate initial approximation and a more precise refinement. Therefore the implementations can be obtained faster and be better optimised.

The aim of this paper is to suggest and illustrate synthesis of speed-independent circuits from the STG-unfolding segment built for their specifications. The method is illustrated on the atomic complex gate per signal architecture and is compared with the existing approaches.

Synthesis of Speed-Independent Circuits

General synthesis approach
We assume that the reader is familiar with the basics of the Petri net theory [7]. A marked Petri net (PN) is a tuple \( N = (P, T, F, m_0) \) where \( P \) and \( T \) are non-empty sets of places and transitions, respectively, \( F \) is a flow relation and \( m_0 \) is an initial marking. A Signal (Transition) Graph (STG) [8, 11] is a tuple \( G = (N, A, L) \) (labelled PN) where \( N \) is a marked PN, \( A \) is a set of signals and \( L : T \to \{+, -\} \times A \) is a labelling function. STGs are a special case of labelled PNs, used for low level descriptions of asynchronous circuits. The set of transition labels represents changes of signals, \(+a_1\) (for up) and \(-a_1\) (for down). Notation \(+a_1\) indicates a transition labelled with a change of \( a_1 \), regardless of the direction of this change.

Conventionally, to obtain an implementation for an STG \( G \) a corresponding SG is built. The SG \( S \), also called a State Transition Diagram (STD), is derived by constructing the reachability graph (representing all reachable markings) of the underlying PN and then assigning binary codes \( v_i \) to each vertex \( s_i \). The binary codes must be assigned consistently, i.e.:

- every arc is labelled with exactly one signal transition, and
- for each pair of states \( s_1 \) and \( s_2 \) connected with an arc labelled with \(+a_1\), the following is true:
  - \( v_1[s] = 0 \) and \( v_2[s] = 0 \) if \( a_1 = +\)
  - \( v_1[s] = 1 \) and \( v_2[s] = 1 \) if \( a_1 = -\)

Once a consistent state assignment was performed, truth tables are obtained for each output signal and an implementation is produced. The process of obtaining a truth table depends on the implementation architecture chosen (for this particular signal).

Correctness criteria for synthesis of speed-independent circuits can be divided into general correctness criteria and architecture specific correctness criteria. The former are behavioural properties of an STG, which characterise an STG to be implementable. In addition to the consistent state assignment, they also include:

- Boundedness, which guarantees that the behaviour specified by an STG can be implemented into a finite size circuit;
• Semi-modularity (also called "output signal persistency"), which implies that excited output signals cannot be disabled by some input signal change and thus cause a hazard.

The latter group of properties is usually checked during the actual logic synthesis process. These are generally referred to as coding conflicts and indicate that although the STG is implementable "in principle", some binary state may be associated with different markings which makes them indistinguishable at the circuit level. The Complete State Coding (CSC) condition introduced in [1] requires any two states with equal binary codes to have the same set of excited output signals. It was shown in [1] that STGs satisfying CSC property are implementable as speed-independent circuits.

An implementation is obtained by building a cover function. A Boolean function with a variable corresponding to each signal is said to be covering a state $s_j$ if it evaluates to TRUE when the variables have the values equal to the elements of binary code $e_j$ assigned to $s_j$. A function $C$ covering a set of states is called a cover function (or simply cover) for this set of states $\{s_j\}$; each term of the cover is called cube.

A cover is not required to be exact, i.e. to cover only the states in $\{s_j\}$. It could be obtained explicitly from their binary codes. However, if a cover is obtained somehow differently (e.g. using an oracle), it may cover some other states. For example, a method described in [6] uses structural information to obtain covers. Such cover is called approximated cover, and needs to be checked for correctness. There are different requirements for correctness of covers according to the implementation architecture chosen.

The following three architecture types are normally considered:

- Atomic complex gate per signal implementation;
- Atomic complex gate per excitation function implementation;
- Atomic complex gate per excitation region implementation.

The first architecture can be considered as a basic type. The other two aim at reducing the size of customised complex gates. In these architectures it is assumed that the output signal is implemented using a memory element. The Set and Reset excitation functions for this memory element are implemented as atomic complex gates (the former) or a network of atomic complex gates (the latter). Depending on which memory element is used, the implementations are divided into (I) Standard C-element implementation, which uses Muller C-element as the memory element, and (II) RS-latch implementation, where an RS-latch is used.

To demonstrate the novel technique we chose the atomic complex gate per signal architecture. Our method, however, can be easily adapted to the other architectures.

Atomic complex gate per signal implementation

This is a basic architecture for speed-independent circuits studied in [1]. The circuit is implemented as a network of atomic gates. Each gate uniquely implements one output signal. Its boolean function can be represented as Sum-Of-Products (SOP) or Sum-Of-Functions (SOF). An example of such gate is shown in Figure 1(b). Each gate is allowed to be sequential (latch), i.e. contain an internal feedback with a zero delay. The delay between its internal "ANDing" and "ORing" parts is also assumed to be negligible. The gate depiction is used to denote the implemented boolean function as the actual implementation is resolved on the transistor level.

Two sets of the reachable states are distinguished in the SG, on-set $On(a)$ and off-set $Off(a)$, which include all states in which the value of the output signal $a$ is true. The remaining (unreachable) subset of combinations of the boolean values of signals forms the Don't care set $(DC-set)$.

The implementation is derived by building the on-set1. Each state can be represented by a term which has $|A|$ variables, each corresponding to one and only one signal $a$. The term becomes TRUE only when the values of the variables are equal to those in the binary code assigned to the state. The cover $C$ for implementation is obtained from the terms included into the on-set. The DC-set can be used for optimising the size of $C$. This is done in standard minimisation tools, such as Espresso [10].

Figure 1: An example of an STG and a corresponding SG.

The synthesis for this architecture is illustrated in Figure 1(c) for an STG shown in Figure 1(a). Suppose that signal $b$ is to be implemented. The on-set of $b$ is found as $On(b) = \{(p_2, p_3), (p_2, p_5), (p_2, p_6, p_8), (p_7, p_8), (p_7, p_9\}$). The cover function $C(b)$ is obtained as $C(b) = ab^{+} + ab^{-} + abc + abc + abc + abc = a + c$. The DC-set in example in Figure 1(c) is empty so no further minimisation can be done.

Obtaining exact covers usually means that all states in the on- or off-set must be known. An approximation algorithm produces approximated covers of the on- and off-sets. Therefore, in this implementation architecture, covers of on- and off-sets must satisfy the following condition:

**Definition 1** Two covers $C^\text{on}(a)$ and $C^\text{off}(a)$ are said to be correct if $C^\text{on}(a)$ and $C^\text{off}(a)$ cover $On(a)$ and $Off(a)$ respectively and $C^\text{on}(a) \cdot C^\text{off}(a) \subseteq DC-set$.

If the covers do not satisfy the above condition, then the approximation is too loose and needs to be refined. If, on the other hand, the covers are exact but still intersect outside the DC-set, then this STG has CSC problem. In this case it should be corrected by changing the specification, e.g. by inserting additional signals.

Slices in STG-unfolding segment

**STG-unfolding segment** Analysis of STGs using STG-unfolding segment was studied elsewhere [9]. An STG-unfolding segment is a tuple $G' = (T', P', F', L')$ where $T'$, $P'$ and $F'$ are sets of transitions, places and the flow relation, respectively, and $L'$ is a labelling function which labels each element of $G'$ as an instance of elements of $G$. $G'$ is a partial order obtained from an STG $G$ by the process of its unfolding which starts from the initial marking. The unfolding process uses the structural properties of the constructed partial order to determine the relations of conflict, concurrency and precedence between instances. These relations are used to decide where to instantiate the next element. The following key notions were introduced in [4]:

- The min-set of transitions needed to fire $t'$, including $t'$, is called local configuration of $t'$ and is denoted as $[t']$.
- A set of place instances reached by firing all transitions in $[t']$ is called postset of $[t']$ and is denoted as $[t']$. Mapping a postset onto places of the original STG is called final state of $[t']$ and gives a marking of the original STG.
- Any non-conflicting and transitively closed set of transitions of $T'$ is called configuration $C$. The postset of a configuration, denoted as $C_{t}$, is found from the postsets of transitions comprising it.

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1 Here and further, for simplicity, it is assumed that the on-set is constructed. Usually, the simplest from the on- and off-sets is chosen for implementation.
The unfolding algorithm examines only states reached through firing of an instance \( t' \) excited by a minimal set of causes. It is based on the fact that no new information about the behaviour of the system can be obtained once the states started repeating. Thus the algorithm constructs no new instances after any instance \( t'_1 \) whose firing reaches an already examined state. Transition instance \( t'_2 \) is called a cutoff transition of the unfolding.

In contrast to PN-unfolding [4], the STG-unfolding takes into account signal interpretation of PN transitions and keeps track of the binary codes reached by transition firing. However, it still examines only a subset of all reachable states and thus is more efficient than SG analysis for a vast number of examples.

Each instance \( t' \) of STG-unfolding segment is assigned with a binary code \( \xi_{t'} \) which is reached by firing transitions in \( \{t'\} \). Similar to its postset, the binary code corresponding to a configuration \( C \) is calculated from \( \xi_{t'} \) of transitions comprising it. It was shown in [9] that all states of the SG are represented in the STG-unfolding segment as postsets of some configuration. For each instance \( t' \) labelled with signal transition \( \ast a_i \), a set of transitions \( \text{next}(t') \) is defined as a set of instances labelled with \( \ast a_i \), reachable from \( t' \) without any intermediate transitions of \( a_i \). Set \( \text{first}(a_i) \) is a set of transitions of \( a_i \) first reached from the beginning of the segment. A special transition, called initial transition, is introduced in the unfolding to represent the initial state of the STG. This transition, denoted as \( \perp \), has a postset which maps onto the initial marking \( m_0 \) and has assigned a binary code \( \xi_{t'} = \perp \) equal to the initial binary state \( v_0 \) of the STG.

It was demonstrated in [9] that an STG-unfolding segment can only be constructed for an STG specification satisfying boundedness and consistent state assignment criteria. The last general correctness criterion, semi-modularity, can be checked on the STG-unfolding segment in linear time.

**Cuts**

To represent a state of SG we define a cut. A cut of STG-unfolding segment is a maximal set of concurrent places \( p' \in P' \). Each cut \( c \) of an STG-unfolding segment thus represents some reachable marking of the original STG. A sequence relation is defined between two cuts \( c_1 \leq c_2 \) if \( \forall p'_i \in c_2 \, \exists p'_j \in c_1 : p'_j \leq p'_i \). For each instance \( t' \) the following four types of cuts are found:

- A **minimal excitation cut** \( c_{\text{exc}}(t') \), which represents a state at which \( t' \) becomes first enabled.
- A **minimal stable cut** \( c_{\text{st}}(t') \), which represents a state which is reached by firing of \( t' \).
- A **maximal excitation cut** \( c_{\text{ex}}(t') \), which represents a state from which, in a correct STG no advancement can be made unless \( t' \) is fired.
- A **maximal stable cut** \( c_{\text{st}}(t') \), which represents a state which is reached after firing of \( t' \) from which firing of any transition leads to a state enabling the next change of the signal \( a_i \) labelling \( t' \).

Each instance of the STG-unfolding segment uniquely identifies \( c_{\text{ex}}(t') \) and \( c_{\text{st}}(t') \) and the sets of \( c_{\text{exc}}(t') \) and \( c_{\text{st}}(t') \). Thus each instance identifies states belonging the subset of the on-set (or off-set) of \( a_i \) which is found for this particular instance.

**Slices**

To represent a (connected) set of states we introduce a notion of a slice of the STG-unfolding segment. A slice of STG-unfolding segment is a set of cuts \( S = \{c_{\text{exc}}(t'), c_{\text{st}}(t')\} \) defined with a min-cut of the slice, \( c_{\text{min}}(t') \), and a set of max-cuts, \( c_{\text{max}}(t') \), such that \( \forall p_i \in S \) the following is true: \( c_{\text{min}}(t') \leq c_i \) and \( \exists c_{\text{max}}(t') \in c_{\text{max}}(t') : c_i = c_{\text{max}}(t') \). No two cuts in the set of max-cuts are sequential.

In other words, a slice is defined between one min-cut and a set of max-cuts. Every cut in between the min-cut and a max-cut is encapsulated in the slice \( S \). Furthermore, for any two cuts \( c_i \) and \( c_j \) encapsulated by \( S \), if \( c_i \prec c_j \), then all cuts between \( c_i \) and \( c_j \) are also encapsulated by \( S \). Since each cut represents some state in the SG, for any two states \( s_i \) and \( s_j \) represented as sequential cuts in a slice, all states on any path from \( s_i \) to \( s_j \) are also represented as cuts encapsulated into \( S \). The number of cuts in the set of max-cuts corresponds to the number of configurations (non-conflicting runs of the STG) which include configuration producing the min-cut. The elements of the STG-unfolding segment, i.e. places and transitions, bounded by instances in min-cut and max-cuts are said to belong to the slice.

A slice represents a subset of reachable states found in the SG for any STG bounded by the cuts defining it. As discussed earlier, the synthesis of speed-independent circuits is based on finding subsets of reachable states. Therefore, slices of the STG-unfolding segment can be used to identify and represent these subsets.

Cuts and slices are illustrated in Figure 2. Consider a cut \( c = (p'_1, p'_0) \) in Figure 2(a). This cut is a minimal excitation cut for the transition \(-c\) and is a minimal stable cut for \(+b\). Another cut, \( c = (p'_3, p'_0, p'_5) \) is a maximal stable cut for transition instance \(+a\). At the same time this is a maximal excitation cut for the instance \(-b\). This example also illustrates the relations between cuts. Intuitively, if a transition \( \ast a_i \) causes \( \ast a_j \), then the minimal stable cut of \( \ast a_j \) is the minimal excitation cut of \( \ast a_i \) and vice versa.

Slices \( S_1 = \{p'_1, \{p'_3, p'_5\}\} \) (Figure 2(b)) encapsulates cut \( c = (p'_4) \). Another slice \( S_2 \) is defined between a min-cut \( (p'_5, p'_6) \) and a set of max-cuts \( \{p'_3, p'_0, p'_5\}\) and includes all cuts between them. It is also possible to define a slice between \( (p'_5, p'_6) \) and \( \{p'_3, p'_0, p'_5\}\). In this case the slice will include all cuts but one enabling \(-a\). This slice, therefore, represents all states at which signal \( a \) is stable at \( "1" \).

Each cut is produced by some configuration of the STG-unfolding segment. Hence, the binary codes of the SG states represented by cuts encapsulated in a particular slice can be recovered by examining its cuts.

**Synthesis from STG-unfolding segment**

**Obtaining exact covers**

First, consider the problem of synthesis from the STG-unfolding segment \( G' \) by finding exact covers for the (on-off)-iset. To implement an output signal of an STG as an atomic gate, its on-set is required. Since its SG is represented as an STG-unfolding segment, the problem is to find a set of slices in this segment which represents all states in the on-set, i.e. an on-set partitioning of \( G' \) for \( a \).

To define each slice we need to identify a min-cut and a set of max-cuts. From all instances in the STG-unfolding segment only instances of \( +a_i \) may change the value of corresponding element in the binary codes. Furthermore, for each instance \( +a_i \) its minimal excitation cut \( c_{\text{exc}}(t') \) represents the first state at which \( +a_i \) becomes excited. Any cut at which \( +a_i \) is excited or stable at \( "1" \) must be sequential to \( c_{\text{exc}}(t') \). A special case is the initial cut.

2 Off-set if an off-set implementation was chosen. In this case instances of \(-a_i \) should be considered.
Figure 3: Illustration of synthesis from the STG-unfolding segment.

transition ⊥ of G'. If in the initial state of the STG the corresponding bit of binary code was "1", then the set first(a_i) will consist of the down instance −a_i. In this case, the minimal stable cut of ⊥ is the first cut from which this slice can be defined. Thus the set of minimal cuts, which is used to define a set of slices, is taken as a set of minimal excitation cuts of instances +a_i and the minimal stable cut of ⊥, if the signal a_i is at "1" in the initial state. Thus a set of transitions, called entry transitions, is identified on the STG-unfolding segment which includes all instances of +a_i and may include ⊥ if a_i is at "1" in the initial state.

For complete definition of each slice we need to determine a set of max-cuts for each slice. The minimal excitation cut of any instance −a_i represents the first state at which −a_i becomes excited. This cut belongs to the off-set.

For each instance +a_i the slice must be bounded by a set of cuts which can be reached from min-cut without exciting −a_i. The slice is bounded by the maximal excitation cuts of immediate predecessors of next(+a_i), i.e. cuts at which an immediate predecessor of a transition from next(+a_i) is the only transition to fire. This is the furthest state to which advancement of the system can be made from +a_i without enabling −a_i. In the case of initial transition the set of max-cuts for the first slice is chosen using first(a_i).

Due to the unfolding algorithm, a particular configuration may contain no instances of −a_i. This may happen if the configuration contains a cutoff transition, or simply leads to a deadlock. In this case the cut reached by such configuration bounds the slice.

Consider synthesising signal 0 from an example in Figure 1. The on-set partitioning of the segment is shown in Figure 3. There are two instances +b' and +b'' and one instance −b. Thus there are two slices S_{on}(+b') = {(p_4), (p_4', p_6)} and S_{on}(+b'') = {(p_4, p_6), (p_4', p_6, p_8)} representing states from the on-set and one slice S_{off} = {(p_5), (p_5')} representing states from the off-set. Once the slices are defined, the set of states represented by these slices is found: On^1(b) = {101, 101, 110, 111} and On^2(b) = {100, 001, 011}. The on-set cover is obtained from states as C_{on} = On^1(b) ∪ On^2(b) = {100, 101, 110, 111, 001, 011} which after standard boolean transformation gives C_{on} = {1, −c, −a, −1} = a + c. If the off-set implementation were chosen, then the cover would be C_{off} = {010, 000} = ac.

Deriving cover approximation from STG-unfolding segment The synthesis procedure described in the previous Sub-section suffers from one drawback. If many concurrent transitions belong to a slice, then obtaining the binary codes for all cuts will suffer from exponential explosion of states. To battle this an approximation method is suggested.

Two types of nodes can be identified in the on-set of signal a_i; those which have +a_i and excited and those at which a_i is stable at "1". The former is traditionally called excitation region (ER) and the latter quiescent region (QR) of rich_a_i. A set of states at which a particular place p_i is marked is called a marked region (MR) of this place. It was pointed out in [6] that a cover for any set of states can be found as an intersection of covers for places which are marked at each state. Thus a set of states at which a particular transition is excited can be found as an intersection of MRs of its preceding places. However, at the unfolding level the instances of transitions are known. The minimal excitation cut c_{erm}(+a_i) for each instance +a_i indicates where this instance becomes first enabled.

Any state reachable from c_{erm}(+a_i), preserving the excitation of +a_i, can only be reached by firing transitions which are concurrent to +a_i. If a signal transition instance +a_i is concurrent to +a_i then the value of its corresponding element in the binary code may take values of both "0" and "1". A cover approximation C_{s}(a_i) is found from the binary code ϕ assigned to the cut c_{erm}(+a_i). Literals corresponding to signals whose instances belong to S_{s}(a_i) and are concurrent to +a_i are substituted by "-" (don't care). Approximation reduces the number of literals in cover C_{s}(a_i) and increases the number of combinations covered by C_{s}(a_i). However, such approximation guarantees that no marking at which +a_i is excited was lost. Furthermore, for a GSC-compliant STG, C_{s}(a_i) will only cover those reachable states where +a_i is excited.

For example, consider calculation of C_{s}(+d') for the instance +d' in Figure 4(b). The binary code corresponding to its minimal excitation cut c_{erm}(+d') = (p_5, p_6, p_8) is excited from the binary code of its local configuration [+d'] as ϕ = {1000000} (the order of signals are abedcf). There are four signals b, c, e, f whose instances belong to the slice and are concurrent to +d'. Thus the ER cover approximation for +d' will be C'(+d') = {1−0−0−0} = adf.

The rest of the states in the on-set which are represented as cuts encapsulated by S_{on}(+a_i) can be approximated by taking cover approximations for MRs of places belonging to S_{on}(+a_i) and sequential to the entry transition of the slice.

For each place p_i its MR approximation cover C_{erm}^+(p_i) is obtained from the binary code ϕ_{+a_i} assigned to its preceding transition. Similar to ER approximation, any marking at which p_i is marked can only be reached by firing transitions concurrent to p_i. Thus literals corresponding to signals whose instances belong to S_{on}(+a_i) and are concurrent to p_i are replaced by "-".

An MR cover approximation for a particular place p_i will cover all states at which p_i is marked with any other concurrent place p_j. Thus only mutually non-concurrent subset of places belonging to S_{on}(+a_i) can be considered. A set of such places is called approximation set P_{a_i}. Furthermore, an MR cover approximation must not cover markings enabling instances t' ∈ next(+a_i). Thus, the MR cover approximation for any such place p_i is found as C(p_i) = ∑ C_{erm}^+(p_i) where C_{erm}^+(p_i) is a cover approximation found for p_i with a set of concurrent signal instances excluding an instance t' immediately preceding t'. To reduce the size of MR cover approximations, it is also convenient to choose P_{a_i} so that it includes one input place from each instance in next(+a_i). The
Cover refinement. Due to the approximated nature of the covers, an on-set cover found from the STG-unfolding segment may implement an incorrect function. Indeed, if an output signal is implemented using an on-set cover approximation which covers a state belonging to the off-set, then the output will change to "1" where it is suppose to be "0". Thus cover approximations obtained using the algorithm described before need to be checked. To check cover correctness both on- and off-set cover approximations are required.

Suppose that both approximated covers for the on- and off-set of an are obtained. Suppose also that their intersection is non-empty. The covers' intersection may only belong to the DC-set. However, to find the DC-set all codes in both on-set and off-set must be known. Therefore, to ensure the covers implement the logic functions correctly we check a stronger condition: approximated covers for on- and off-set are said to be correct if their intersection is empty. The approximation produces semi-optimised covers. Exact covers have their intersection empty by construction. Therefore, if the covers' intersection is non-empty, then they need to be refined until their intersection becomes empty, possibly covering the exact covers. Thus the use of a stronger condition only affects the quality of optimisation rather than correctness of covers. If after complete refinement on- and off-set covers still intersect, then this STG has a CSC problem and cannot be implemented without changes to the specification. Correct refined covers can be optimised using any known minimisation technique.

The pseudo-code of the algorithm for deriving covers for on and offsets is shown in Figure 5. The initial on- and off-set cover approximations are found as described in the previous Subsection. If the approximated covers' intersection is not empty, then these covers are refined. Only concurrency relation was used for finding approximated covers. Other relations between transitions concurrent to \( a' \) were ignored. The general idea behind refinement is that using these relations some of the informations about the cover is restored. Covers are refined until "they are good enough", i.e. covers' intersection becomes empty.

The on- and off-set covers' intersection may become non-empty due to approximation of MR cover for some places in the approximation set. These MR cover approximations may intersect with the ER cover approximations of some instances of the opposite signal transition. In this case only cover approximations for these places (but not all in the approximation set) and the instance of opposite signal transition need to be refined. The set of signals \( S|g \) which cause the intersection is also known. These are exactly those signals whose value is undefined in one of the cubes \( B \in C^a \). Thus we need to consider a problem of refining a cover approximation for an element \( x' \) of STG-unfolding segment with \( S|g \).

For each implementable signal \( a \), do
- Find sets of on- and off-slices \( S^a_{On} \) and \( S^a_{Off} \)
- for each slice \( S^a_{On} \)
  - Find approximation set \( P^a \)
  - \( C^a_{On} = C^a_{On}(a) + \sum C^a_{On}(p_i), p_i \in P^a \)
- for each slice \( S^a_{Off} \)
  - Find approximation set \( P^a \)
  - \( C^a_{Off} = C^a_{Off}(a) + \sum C^a_{Off}(p_i), p_i \in P^a \)
- end do
  - \( P^a \) initial approximations found \( \forall a \)
- while \( C^a_{On} \cdot C^a_{Off} \neq \emptyset \)
  - for each \( C^a_{On}(p_i) \) and \( C^a_{Off}(p_i) \)
    - Find the set of offending signals \( S|g \)
    - Choose offending signal \( a_j \) from \( S|g \)
    - Find refining set \( P^a \) for \( p_i \) w.r.t. \( a_j \)
    - \( C^a_{new}(p_i) = C^a_{new}(p_i) + \sum C^a_{new}(p_k) \) \( p_i \in P^a \)
    - Find refining set \( P^a \) for \( p_i \) w.r.t. \( a_j \)
    - \( C^a_{new}(p_i) = C^a_{new}(p_i) + \sum C^a_{new}(p_k) \) \( p_i \in P^a \)
  - end do
- end do

Figure 5: Algorithm for deriving on- and off-set cover approximations from STG-unfolding segment


\[ V^4 \in P^4 \models x' \] Furthermore, the set is chosen so that for at least one signal \( a \) from \( S|g \) for each its instance \( t^i \in S^a_{On}(a') \) one of the successors of \( t^i \) is in \( P^4 \). Thus each refining step will refine at least one signal from \( S|g \). A refined cover \( C^a_{new}(x') \) is obtained from the old approximation as:

\[ C^a_{new}(x') = C^a_{new}(x') + \sum C^a_{new}(p_k), p_k \in P^4 \]

where \( V^4 \in P^4 \) is a restricted MR cover for \( p_k \) where only those literals are set to "1" whose instances \( t^i | p_k \) belong to \( S^a_{On}(a') \) and are successors of \( a' \).

Informally, at each step the refinement procedure restores the marking component of reachable states represented by the slice. It finds a set of places which can be marked together with each already partially restored marking. The cover function is then changed reflecting the fact that partially restored markings now include found places. Thus in the end, when the procedure terminates, the covers correspond to fully restored markings and cover only states with these marking components.

Since each step refines the value of at least one variable and the set of signals is finite, the refinement procedure will terminate in finite number of steps producing an exact cover for the states represented the slice \( S^a_{On}(a') \).

Consider a fragment of STG-unfolding segment shown in Figure 4(c). Suppose that on-set cover approximation \( C^a_{On} \) found with approximation set \( P^a \) intersects with \( C^a_{Off} \) for some signal. Suppose also that a cube \( B = d\bar{e} \) which is an MR cover approximation of place \( p_k \) causes this non-empty intersection. The set of offending signals is found as \( S|g = \{a, b, c\} \). Let \( a \) be the signal chosen for refinement. Its only instance which should be used in refinement is \( a' \). A refinement set is chosen as \( P^a = \{p_k, p_4, p_7, p_5\} \). Consider calculation of the restricted MR cover approximation for \( p_k \). The only instances which can be used in approximation is \( a' \) as other concurrent instances, \( a' \) and \( d \), precede \( p_k \). Thus \( C^a_{On}(p_k) = \{101-1\} \) (the order of signals is \( abcd \)). Similar, MR cover approximations are found for other places in \( P^4 \). The refined cover approximation is thus found as:

\[ C^a_{new}(p_k) = \{(-10)1 \} \cup \{1101\} \cup \{1101\} \cup \{0111\} \}

The resulting cover is an exact cover for MR place \( p_k \). Note that if simply MR cover approximation \( C^a_{On}(p_k) = be \) were chosen for \( p_k \), then refinement would not refine \( a' \).
count for all three tools was the same. Both SIS and Petriy exhibit doubly exponential growth of time taken. The first dependency is due to the state space explosion, the second is due to the exponential complexity of the exact synthesis process used in both tools. In addition, we synthesised a Counterflow pipeline specification [11] which has 34 signals. From the existing tools, only Petriy was able to synthesise it taking more than 24 hours. At the same time PUNT was able to synthesise it in under 2 hours thus giving an order of magnitude gain in speed. This is shown on the graph as a circled dot.

Conclusions

In this paper we presented a new method for synthesis of speed independent circuits. Our approach is based on the STG-unfolding segment. It uses the segment as a model from which an implementation is obtained. As the size of the STG-unfolding segment is often smaller than the size of the SG, it is possible to synthesise specifications of larger sizes. In addition, due to the smaller size of the semantic model, the implementation can be achieved faster on a number of moderate sized examples. We demonstrated applicability of our method on an existing set of benchmarks.

Future development of this method can be directed into exploring heuristics for the refinement procedure, which is the core of our method. In addition, this method can be adapted to the other implementation architectures. In this case, the approximation will be used to obtain the excitation functions for memory elements by finding the slices corresponding to the required regions of the SG. Furthermore, the method can be enhanced by accommodating checks for weaker correctness conditions for approximated covers.

REFERENCES


